IQS7219A DATASHEET

A Versatile Proximity Sensing Device for High Performance and Low Power Application. The device is focused on proximity and touch applications with direct output requirements. Up to 2 channels can be configured in a range of available sensing modes

1 Device Overview

1.1 Main Features

- Highly flexible ProxFusion® device
- 2 configurable channels
  - Each channel can pair multiple sensor connections. (see Figure 1.1).
- Self/Mutual capacitive sensors
- Sensor flexibility
  - Automatic sensor tuning for optimum sensitivity
  - Internal voltage regulator
  - Reference capacitor
  - On-chip noise filtering
  - Detection debounce and hysteresis
  - Wide range of capacitance detection
- Proximity Sensing
  - High SNR for proximity sensing
  - High parasitic load capability (400pF)
- Variance detection
  - Calculate signal variance
  - Triggers based on signal variance level
  - Variance estimates user interaction level (user movement magnitude)
- Design simplicity
  - PC GUI for obtaining optimal on-chip settings
  - One-time settings programming(during MP)
- 3x GPIO's to output status flags from any channel
- Automated system power modes for optimal response vs consumption
- I^2C communication interface with IRQ/RDY(up to fast plus -1MHz)
- Standalone, event mode (RDY based), streaming mode (RDY based) or polling communication options
- Fully customizable standalone user interface due to programmable memory
- Supply Voltage 1.8V(-5%)to 3.5V
- Small packages:
  - WLCSP18 (1.62x 1.62x0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch

RoHS2 Compliant

WLCSP18 & QFN20 package representation only

1.2 Applications

- SAR-limiting proximity sensing
- Proximity Backlighting
- Presence detection

1.3 Block Diagram

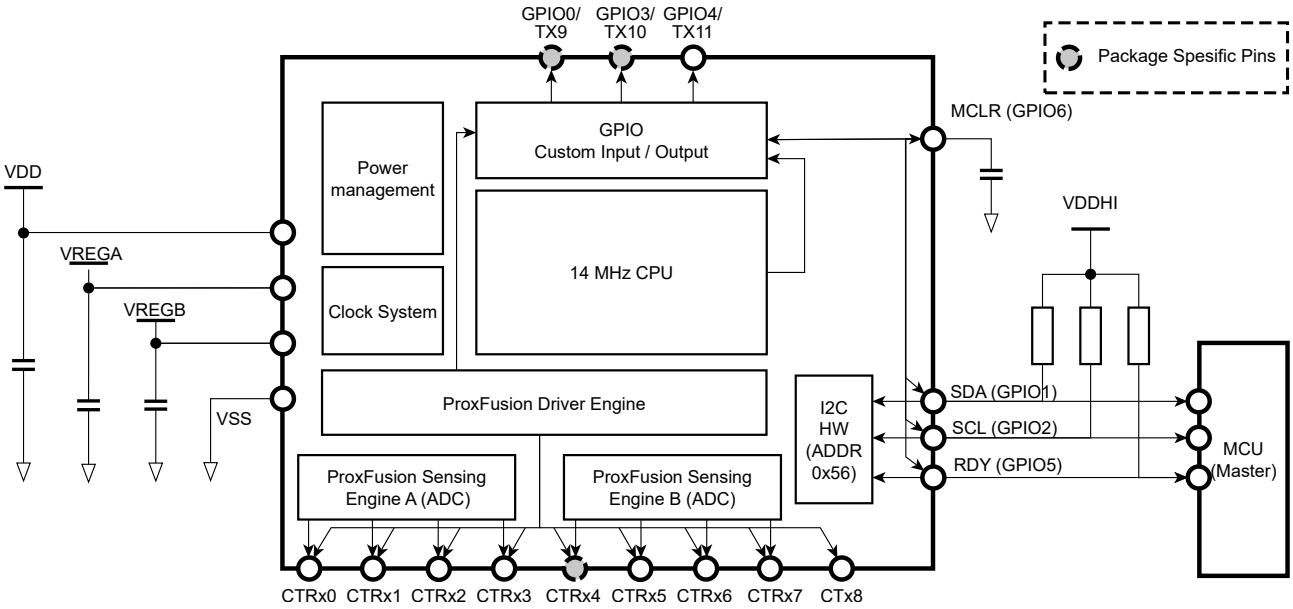


Figure 1.1: Functional Block Diagram[1]

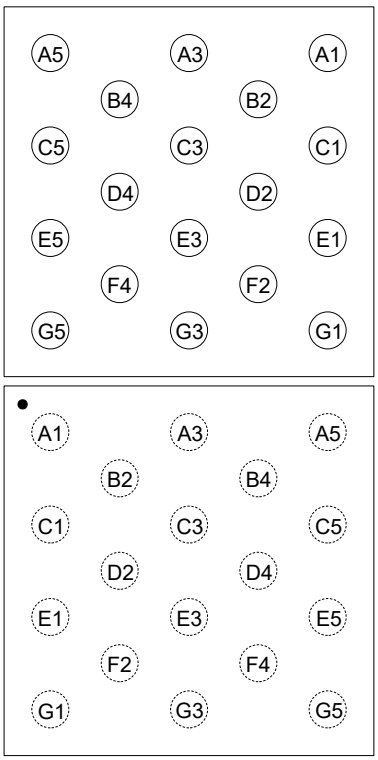
[1] WLCSP18 packages do not have a CRx4 and combines GPIO0 and GPIO3

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

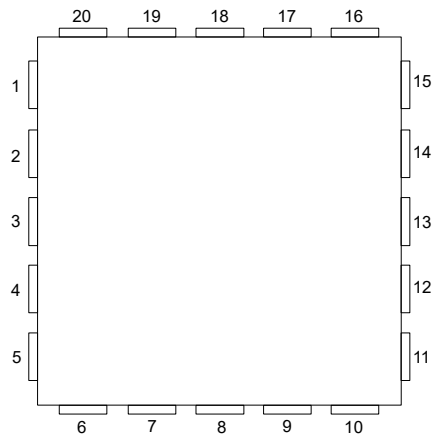
Table 2.1: 18-pin WLCSP18 Package (Bottom/Ball-side View)



Pin no.	Signal
A5	GPIO6 / MCLR
A3	SCL/ GPIO2
A1	CTx9/CTx10/GPIO0/GPIO3[2]
B4	SDA/GPIO1
B2	CTx11/GPIO4
C5	VDD
C3	RDY/ GPIO5
C1	CTx8
D4	VSS
D2	CRx2/CTx2
E5	VREGD
E3	CRx1/CTx1
E1	CRx6/CTx6
F4	CRx0/CTx0
F2	CRx5/CTx5
G5	VREGA
G3	CRx3/CTx3
G1	CRx7/CTx7

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6
2	VREGD	12	CRx7
3	VSSD & VSSA	13	CTx8
4	VREGA	14	GPIO0
5	CRx0	15	GPIO3
6	CRx1	16	GPIO4
7	CRx2	17	GPIO5
8	CRx3	18	GPIO2
9	CRx4	19	GPIO1
10	CRx5	20	GPIO6

Area name	Signal name
Tab	Ground

[2]Please note that CTx9 and CTx10 are connected together in the WLCSP18 package

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no. WLCSP18	Pin no. QFN20	Signal name	Signal type[3]	Buffer type	Power source
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSSA & VSSD	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	GPIO0/CTx9	Digital/Prox		VDD/VREGA
B4	19	SDA/GPIO1	Digital		VDD
A3	18	SCL/GPIO2	Digital		VDD
A1	15	GPIO3/CTx10	Digital/Prox		VDD/VREGA
B2	16	GPIO4/CTx11	Digital/Prox		VDD/VREGA
C3	17	RDY/GPIO5	Digital/Prox		VDD
A5	20	MCLR/GPIO6	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no. WLCSP18	Pin no. QFN20	Pin type	Description
ProxFusion®	CRx0	F4	5	IO	ProxFusion® channel
	CRx1	E3	6	IO	
	CRx2	D2	7	IO	
	CRx3	G3	8	IO	
	CRx4	-	9	IO	
	CRx5	F2	10	IO	
	CRx6	E1	11	IO	
	CRx7	G1	12	IO	
	CTx8	C1	13	IO	
	CTx9/ GPIO0	A1	14	IO	CTx9 pad
	CTx10/GPIO3	A1	15	IO	CTx10 pad
	CTx11/GPIO4	B2	16	IO	CTx11 pad
	CTx12/GPIO5	C3	17	IO	Input filter disabled for external clock input.
GPIO	MCLR/ GPIO6	A5	20	IO	Active pulldown, 200k resistor to VDD, Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I^2C	SDA/GPIO1	B4	19	IO	I^2C Data
	SCL/GPIO2	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSSA/VSSD	D4	3	P	Analog/Digital Ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[3] Signal Types: I = Input, O = Output, I/O = Input or Output

2.5 Reference Schematic

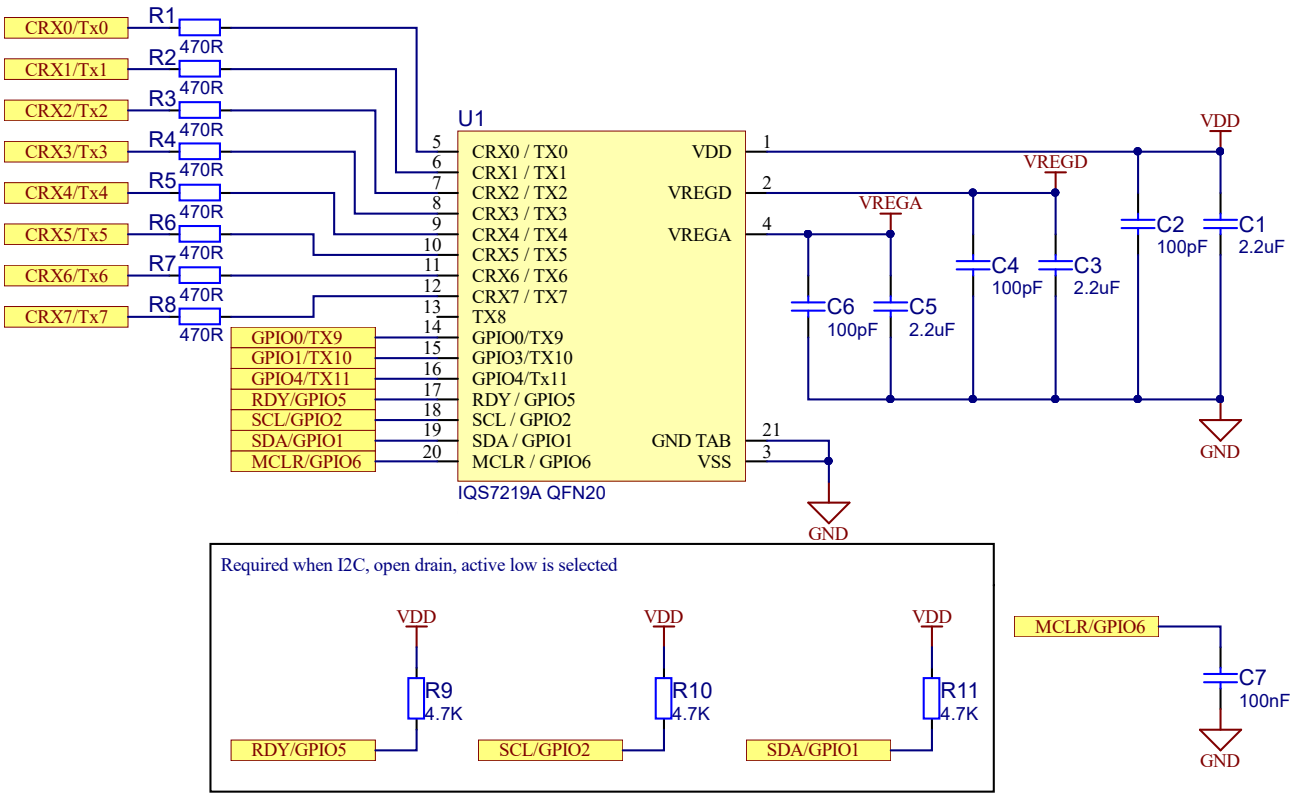


Figure 2.1: IQS7219A Reference Schematic

2.6 Single Channel Wake-up UI Summary

The IQS7219 achieves an effective power consumption vs performance ratio for applications where battery size is limited. This is done via an integrated power mode switching that also switches the state of the sensor pins.

Wake-up source	Description	Advantage
Trackpad pattern	The full trackpad design is used as a single touch key for wake-up	Extra sensing pad for larger trackpad or other sensing options
Touch button	A single button is defined separate from the trackpad area	Dedicated touch area for screen wake-up (less unintended screen wake-up triggers)

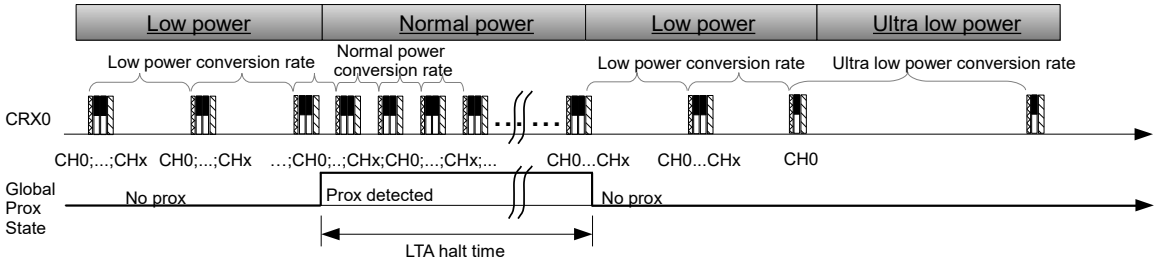


Figure 2.2: Power Mode Switching Timing Diagram

Table 2.5 below describes the power modes along with the touch UI state in relation to the channels shown in Figure 2.2.

Table 2.5: Power Modes and Corresponding Touch UI

Power mode step	Description	Channel details
Automatic mode stepping (default)	Timer determines a constant state & steps to a lower power state automatically	
ULP (Ultra low power)	"Single channel active" state (CH0) where all channels are updated at a much slower rate	CH0 only (Trackpad/touch button wake-up) (CH1 .. CHx updated periodically) Wear detect state updated Force touch state updated
LP (Low power)	Multi-channel state where all channels are sampled at a custom lower power rate - ideal for slowly tracking changes during active use	CH0 to CHx sampled
NP (Normal power)	Full power state where all channels are sampled at optimal rate for the application	CH0 to CHx sampled

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T_{stg}	-40	85	℃

3.2 ESD Rating

Table 3.2: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[4]	± 4000	V

3.3 Recommended Operating Conditions

Table 3.3: Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14MHz F_{OSC} = 18MHz	 1.71 2.2		 3.5 3.5	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14MHz F_{OSC} = 18MHz		 1.53 1.75		V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14MHz F_{OSC} = 18MHz		 1.59 1.8		V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	-40	25	85	℃
C_{VDD}	Recommended capacitor at VDD	1	2	10	µF
C_{VREGA}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	1	2	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	1	2	10	µF
$Cx_{\_SELF-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1	-	400[5]	pF
$Cm_{\_CTX-CRX}$	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-cap mode)	0.2	-	9[5]	pF
$Cp_{\_CRX-VSS-1M}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @f_{xfer}=1MHz)			100[5]	pF
$Cp_{\_CRX-VSS-4M}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f_{xfer}=4MHz sensing))			25[5]	pF
$\frac{Cp_{CRX-VSS}}{Cm_{CTX-CRX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode [6]	10		20	n/a
$RCx_{\_CRX/CTX}$	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0[7]	0.47	10[8]	kΩ
$RCx_{\_SELF}$	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[7]	0.47	10[8]	kΩ

3.4 Current Consumption

Power mode	Active channels	Voltage (V)	Current [µA]
Active Mode	Single Channel	3.5	76
Active Mode	Single Channel	1.7	76

[4]JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

[5]RCx = 0 Ω

[6]Please note that the the maximum values for Cp and Cm are subject to this ratio

[7]Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

[8]Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} x C_{max} = $\frac{1}{(6x f_{xfer})}$ where "C" is the pin capacitance to Vss.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) - slope >100V/s	1.040	1.353	1.568	V
V_{VREG}	Power-up/down level (Reset trigger) - slope >100V/s	0.945	1.122	1.304	V

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)VDD\_HI}$	MCLR Input high level voltage	VDD = 3.3V	VSS-0.3	-	1.05	V
$V_{IL(MCLR)VDD\_LOW}$	MCLR Input low level voltage	VDD = 1.7V	VSS-0.3	-	0.75	V
$V_{IH(MCLR)VDD\_HI}$	MCLR Input high level voltage	VDD = 3.3V	2.25	-	VDD_HI+0.3	V
$V_{IH(MCLR)VDD\_HI}$	MCLR Input high level voltage	VDD = 1.7V	1.05	-	VDD_LOW+0.3	V
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	VDD = 3.3V	-	-	15	ns
$t_{PULSE(MCLR)}$	MCLR input pulse width - no trigger	VDD = 1.7V			10	ns
$t_{TRIG(MCLR)}$	MCLR input pulse width - ensure trigger	VDD = 3.3V, VDD = 1.7V	250	-	-	ns

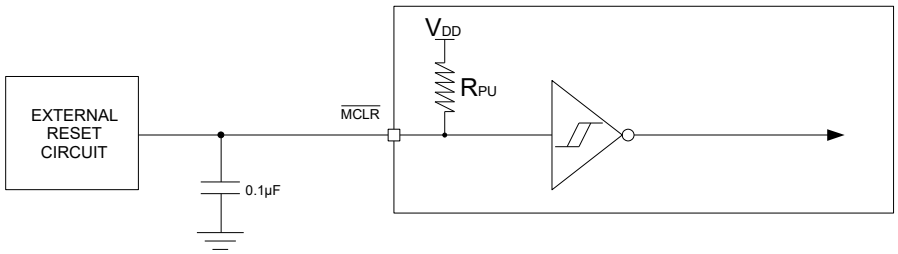


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{SYS})	42	500-1500	5000	kHz
f_{OSC}	Master CLK frequency tolerance 14MHz	13.23	14	14.77	MHz
f_{OSC}	Master CLK frequency tolerance 18MHz	17.1	18	19.54	MHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	GPIO1 & GPIO2 Output low voltage	I_{sink} = 20mA			0.3	V
V_{OL}	GPIO0,3,4,5 Output low voltage	I_{sink} = 10mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20mA	VDD - 0.2			V
V_{IL}	Input low voltage		VDD * 0.3			V
V_{IH}	Input high voltage				VDD * 0.7	V
C_{b_max}	GPIO1 & GPIO2 maximum bus capacitance				550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Test Conditions	VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		1.8V, 3.3V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		1.8V, 3.3V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START		1.8V, 3.3V	0.26			µs
$t_{HD,DAT}$	Data hold time		1.8V, 3.3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V, 3.3V	50			ns
$t_{SU,STO}$	Setup time for STOP		1.8V, 3.3V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		1.8V, 3.3V	50			ns

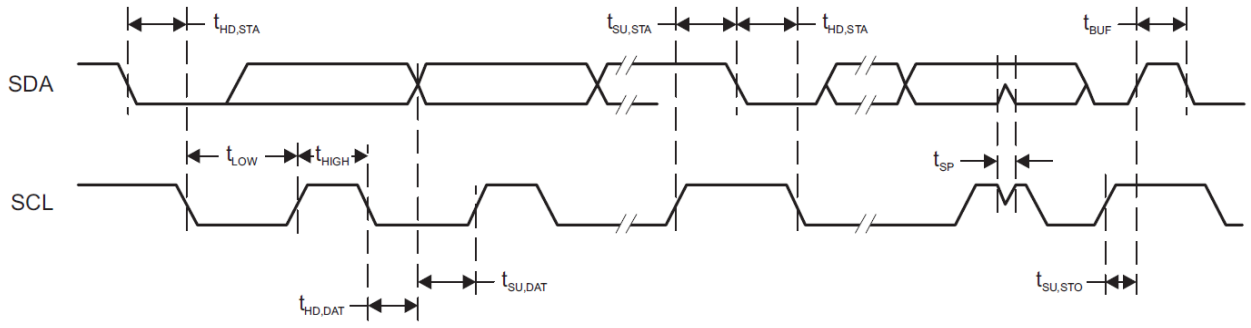


Figure 4.2: I²C Mode Timing Diagram

5 I²C Interface

5.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The communications interface of the IQS7219A supports the following:

- *Fast-mode-plus* standard I2C up to 1MHz.
- Streaming data as well as event mode.
- The master may address the device at any time. If the IQS7219A is not in a communication window, address polling will be acknowledged immediately with minimal clock stretching.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7219A implements 16bit addressing with 2 bytes at each address. Two consecutive read-/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" and "byte 1".

5.2 I²C Address

When in debug or I²C mode, the IQS7219A has a fixed I2C address of 0x56.

Other address options exist on special request. Please contact Azoteq.

5.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

5.4 Memory Map Addressing

5.4.1 16-bit Address

The memory map implements a 16-bit addressing scheme for the required user data.

5.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data.
The 16-bit data is sent in little endian byte order (least significant byte first).

5.6 Terminate Communication

A standard I²C STOP ends the current communication window.

5.7 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected.

6 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)		Notes
0x00 - 0x09	Version details		See Table A.1
	Device Status		
0x10	System Fields		See Table A.2
0x11	PXS Status		See Table A.3
	Channel Counts		
0x12	Channel 0 Filtered		16-bit value
0x13	Channel 0 LTA		
0x14	Channel 1 Filtered		
0x15	Channel 1 LTA		
0x16	Channel 0 Variance LSB		See Table A.4
0x17	Channel 0 Variance MSB		
0x18	Channel 1 Variance LSB		See Table A.4
0x19	Channel 1 Variance MSB		
0x1A	Channel 0 Raw		16-bit value
0x1B	Channel 1 Raw		
	ATI Parameters		
0x20	Reserved	Channel 0 Course Multiplier	4-bit value
0x21	Reserved	Channel 0 Course Divider	5-bit value
0x22	Reserved	Channel 0 Fine Divider	5-bit value
0x23	Reserved	Channel 0 ATI Compensation Divider	5-bit value
0x24	Channel 0 ATI Compensation		12-bit value
0x25	Reserved	Channel 1 Course Multiplier	4-bit value
0x26	Reserved	Channel 1 Course Divider	5-bit value
0x27	Reserved	Channel 1 Fine Divider	5-bit value
0x28	Reserved	Channel 1 ATI Compensation Divider	5-bit value
0x29	Channel 1 ATI Compensation		12-bit value
	PMU and System Settings		
0x80	System Setup and Commands		See Table A.5
0x81	Watchdog Timeout		See Table A.6
0x82	ATI Mode - Retry ATI on error period		16-bit value (ms)
0x83	ATI Mode - Minimum ATI sample period		16-bit value (ms)
0x84	Normal Power Mode Timeout		16-bit value (ms)
0x85	Normal Power Mode Report Rate		16-bit value (ms)
0x86	Low Power Mode Timeout		16-bit value (ms)
0x87	Low Power Mode Report Rate		16-bit value (ms)
0x88	Ultra Low Power Mode Timeout		16-bit value (ms)
0x89	Ultra Low Power Mode Report Rate		16-bit value (ms)
	PXS Settings		
0x8A	Cycle 0 Channel Select		See Table A.7
0x8B	Cycle 1 Channel Select		See Table A.7
0x8C	Projected and Self Mode Settings		See Table A.8
	Channel 0 Detection Settings		
	Halt Detection Settings		
0x90	Active State Timeout		16-bit value (ms)
0x91	Hysteresis		$\frac{Threshold}{2^{16}}$
0x92	Threshold		$\frac{LTA}{256} * 16bitvalue$
0x93	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0x94	Reserved	GPIO Select	See Table A.10
	Proximity Detection Settings		
0x95	Active State Timeout		16-bit value (ms)
0x96	Hysteresis		$\frac{Threshold}{2^{16}}$
0x97	Threshold		$\frac{LTA}{256} * 16bitvalue$
0x98	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0x99	Reserved	GPIO Select	See Table A.10

	Touch Detection Settings		
0x9A	Active State Timeout		16-bit value (ms)
0x9B	Hysteresis		$\frac{Threshold}{2^{16}}$
0x9C	Threshold		$\frac{LTA}{256} * 16bitvalue$
0x9D	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0x9E	Reserved	GPIO Select	See Table A.10
	Channel 0 PXS and ATI Settings		
0xA0	General Settings		See Table A.11
0xA1	Filter Betas		See Table A.12
0xA2	Conversion Period	Frequency Fraction	See Table A.13
0xA3	CRx Selection		See Table A.14
0xA4	CTx Selection		See Table A.15
0xA5	ATI Base		16-bit value
0xA6	ATI Target		16-bit value
0xA7	re-ATI Band		16-bit value
0xA8	ATI Mode		See Table A.16
0xA9	Course Divider Preload	Fine Divider Preload	8-bit value
0xAA	Compensation Preload		16-bit value
0xAB	Variance Threshold		16-bit value
	Channel 1 Detection Settings		
	Halt Detection Settings		
0xB0	Active State Timeout		16-bit value (ms)
0xB1	Hysteresis		$\frac{Threshold}{2^{16}}$
0xB2	Threshold		$\frac{LTA}{256} * 16bitvalue$
0xB3	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0xB4	Reserved	GPIO Select	See Table A.10
	Prox Detection Settings		
0xB5	Active State Timeout		16-bit value (ms)
0xB6	Hysteresis		$\frac{Threshold}{2^{16}}$
0xB7	Threshold		$\frac{LTA}{256} * 16bitvalue$
0xB8	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0xB9	Reserved	GPIO Select	See Table A.10
	Touch Detection Settings		
0xBA	Active State Timeout		16-bit value (ms)
0xBB	Hysteresis		$\frac{Threshold}{2^{16}}$
0xBC	Threshold		$\frac{LTA}{256} * 16bitvalue$
0xBD	Debounce Deactivation Threshold	Debounce Activation Threshold	See Table A.9
0xBE	Reserved	GPIO Select	See Table A.10
	Channel 1 PXS and ATI Settings		
0xC0	General Settings		See Table A.11
0xC1	Filter Betas		See Table A.12
0xC2	Conversion Period	Frequency Fraction	See Table A.13
0xC3	CRx Selection		See Table A.14
0xC4	CTx Selection		See Table A.15
0xC5	ATI Base		16-bit value
0xC6	ATI Target		16-bit value
0xC7	re-ATI Band		16-bit value
0xC8	ATI Mode		See Table A.16
0xC9	Course Divider Preload	Fine Divider Preload	8-bit value
0xCA	Compensation Preload		16-bit value
0xCB	Variance Threshold		16-bit value

7 Applications, Implementation and Layout

7.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 2.2-µF plus a 100-pF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

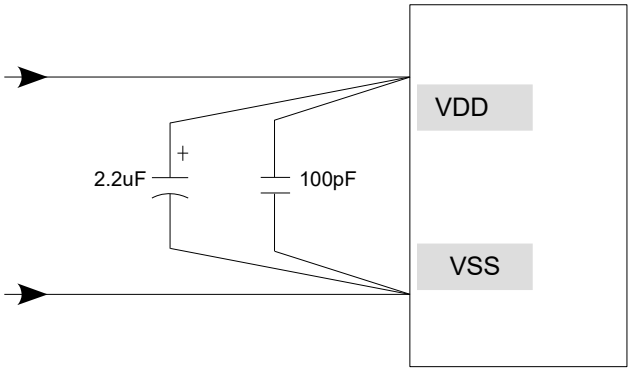


Figure 7.1: Recommended Power Supply Decoupling

7.1.2 Transient Signal Management

During power up, power down, and device operation, VDD must not exceed the absolute maximum ratings. Exceeding the specified limits may cause malfunction of the device.

7.1.3 ProxFusion® Peripheral

This section provides a brief introduction to the ProxFusion® technology with examples of PCB layout and performance from a design kit. Please contact Azoteq for more details on design variables not covered here.

7.1.4 VREG

The VREG pin requires a 2.2-µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the microcontroller. The figure below shows an example layout where the capacitor is placed close to the IC.

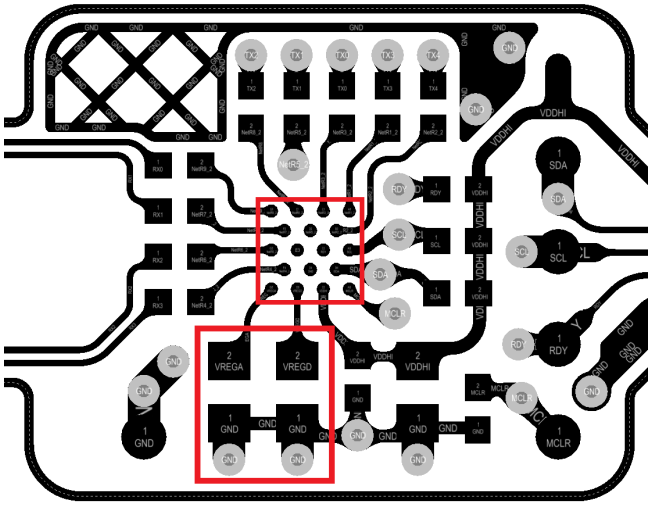


Figure 7.2: VREG Capacitor Placement Close to IC

7.1.5 ESD Protection

Typically, the laminate overlay provides several kilovolts of breakdown isolation to protect the circuit from ESD strikes. More ESD protection can be added with a series resistor placed on each channel used. A value of 470 Ω is recommended.

7.1.6 Self-capacitance Electrode Design

Self-capacitance electrodes are characterized by having only one sensing pin from the IC that both excites and measures the capacitance. The capacitance being measured is between the electrode and circuit ground, so any capacitance local to the PCB or outside of the PCB (a touch event) influences the measurement.

For PCB layout design it is important to minimize local parasitic capacitances while shielding (with circuit GND) the self-capacitance traces against mechanical changes, induced noise and temperature effects of the board material. Minimize the local parasitic capacitances in order to maximize the effect of external capacitances (proximity and touch effects). To minimize parasitic effects on the PCB, the ground pour on the bottom layer is hatched and there is no pour directly below the electrode: 1.27mm spacing between the electrode and ground fill.

7.1.7 ATI (Auto Tuning Implementation)

The ATI process adjusts three values (Coarse multiplier, Fine multiplier, Compensation) using two parameters per plate (ATI base and ATI target). The ATI process is used to ensure that the sensor's sensitivity is not severely affected by external influences (Temperature, voltage supply change, etc.). For a detailed description of ATI, please contact Azoteq.

8 Ordering Information

8.1 Ordering Code

IQS7219A zzz ppb

IC NAME	IQS7219A	=	IQS7219A	
POWER-ON CONFIGURATION	zzz	=	000	Reserved
		=	102	Sensitive[9]
		=	103	Sensitive Max[10]
		=	103	Sensitive + Movement (variance)
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Figure 8.1: Order Code Description

8.2 Top Marking

8.2.1 WLCSP18 Package

IQS
7219B
pppxx
•

Product Name
ppp = product code
xx = batchcode

8.2.2 QFN20 Package Marking Option 1

•
IQS
7219B
pppxx

Product Name
ppp = product code
xx = batchcode

8.2.3 QFN20 Package Marking Option 2

•
IQS
721xy
pppxx

Product Name
ppp = product code
xx = batchcode

9 Package Specification

9.1 Package Outline Description - WLCSP18

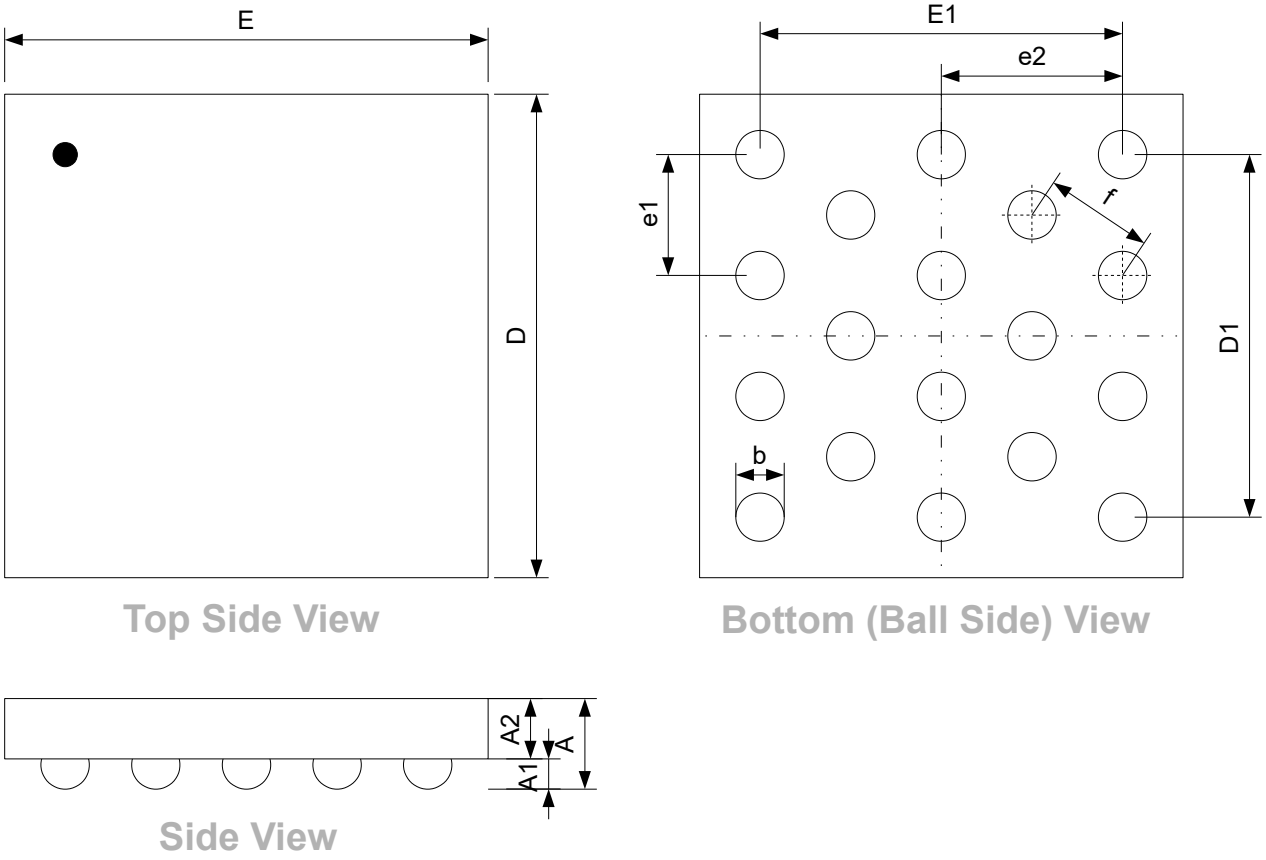


Figure 9.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Table 9.1: WLCSP (1.62x1.62) - 18 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.525±0.05	E	1.620±0.015
A1	0.2±0.02	E1	1.2
A2	0.3±0.025	e1	0.4
b	0.260±0.039	e2	0.6
D	1.620±0.015	f	0.36
D1	1.2		

9.2 Package Outline Description - QFN20

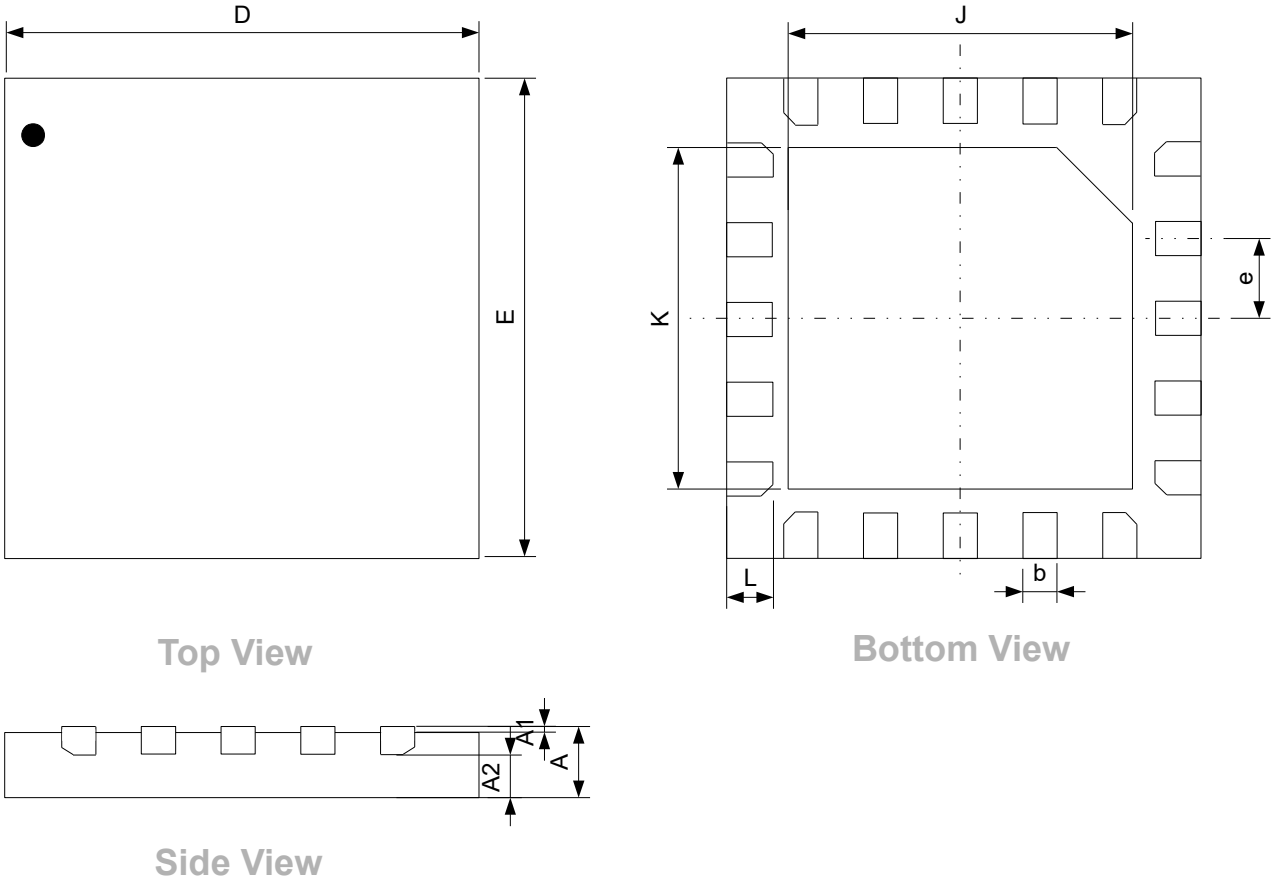


Figure 9.2: QFN (3x3)-20 Package Outline Visual Description

Table 9.2: QFN (3x3)-20 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.5±0.1	E	3
A1	0.035±0.05	e	0.4
A2	0.3	J	1.7±0.1
A3	0.203	K	1.7±0.1
b	0.2±0.05	L	0.4±0.05
D	3		

9.3 Moisture Sensitivity Levels

Contact Azoteq

9.4 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Table A.1: Version Information

Address	Category	Name	Value
0x00	Application Version Info	Product Number	685
0x01		Major Version	1
0x02		Minor Version	12
0x03		Patch Number (Commit hash)	Value between 0 and 65536
0x04			

Table A.2: System Fields

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Mode		Device Reset	Res	ATI Error	ATI Active	Reserved			Power Event	ATI Event	Res	Prox Event	Halt Event

- Bit 12-13: **Power Mode**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra-Low Power
- Bit 11: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 9: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 8: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 4: **Power Event**
  - 0: No power event occurred
  - 1: Power event occurred
- Bit 3: **ATI Event**
  - 0: No ATI event occurred
  - 1: ATI event occurred
- Bit 1: **Proximity Event**
  - 0: No Proximity event occurred
  - 1: Proximity event occurred
- Bit 0: **Halt Event**
  - 0: No Halt event occurred
  - 1: Halt event occurred

Table A.3: PXS Status

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved										CH1 Prox	CH1 Halt	Reserved		CH0 Prox	CH0 Halt

- Bit 5: **CH1 Proximity**
  - 0: No Proximity event occurred on Channel 1
  - 1: Proximity event occurred on Channel 1
- Bit 4: **CH1 Halt**
  - 0: No Halt event occurred on Channel 1
  - 1: Halt event occurred on Channel 1
- Bit 1: **CH0 Proximity**
  - 0: No Proximity event occurred on Channel 0
  - 1: Proximity event occurred on Channel 0
- Bit 0: **CH0 Halt**

- 0: No Halt event occurred on Channel 0
- 1: Halt event occurred on Channel 0

Table A.4: Channel Variance

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16 Bit Value															

> Bit 0-15: **Channel Variance**
  - 0: Variance channel is disabled and signal variance will not reset timer
  - 16-Bit value: Signal variance trigger size
> Bit 0: **PXS Mode**
  - 0: Self-Capacitance
  - 1: Projected Capacitance

Table A.5: System Setup and Commands

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						NP Segment Rate		Interface Selection		Power Mode Selection		Reseed	ATI	Reset	Ack reset

> Bit 8-9: **Normal Power Segment Rate**
  - 00: Every 2 Cycles
  - 01: Every 4 Cycles
  - 10: Every 16 Cycles
  - 11: Every 32 Cycles
> Bit 6-7: **Interface Selection**
  - 00: I^2C streaming
  - 01: I^2C event mode
  - 10: Standalone
  - 11: Standalone + POR I^2C
> Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Automatic power mode switching
> Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
> Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
> Bit 1: **Reset Device Command**
  - 0: Do not reset device
  - 1: Reset device
> Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.6: Watchdog Timer Buffer

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Watchdog Timer Buffer [10ms]							

> Bit 0 - 7: **Watchdog Timer Buffer**
  - Watchdog timer is dynamically set according to sample period
  - Watchdog timer = 8-bit Watchdog timer buffer value x 10ms (minimum 10ms) + sample period

Table A.7: Cycle Settings

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Selected Channel Number								Reserved							PXS Mode

- Bit 18-15: **Selected Channel Number**
  - 0: Channel 0
  - 1: Channel 1
  - 256: None
- Bit 0: **PXS Mode**
  - 0: Self-Capacitance
  - 1: Projected Capacitance

Table A.8: Projected and Self Capacitance Settings

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Self-Capacitance								Projected Capacitance							
Res	Res set 0	RF Filter	CS 80pF	Reserved		Max Counts		Res	Res set 0	RF Filter	CS 80pF	Projected Bias Select		Max Counts	

- Bit 13 & Bit 5: **RF Filter**
  - 0: filter disabled
  - 1: filter enabled
- Bit 12 & Bit 4: **Cs 80pF cap**
  - 0: 40pF
  - 1: 80pF
- Bit 8-9 & Bit 0-1: **Maximum Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-3: **Projected Bias Selection**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.9: Debounce Thresholds

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Debounce Deactivation Threshold								Debounce Activation Threshold							

- Bit 8-15: **Debounce Deactivation Threshold**
  - 8bit value
- Bit 0-7: **Debounce Activation Threshold**
  - 8bit value

Table A.10: GPIO Selection

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								GPIO Select							

- Bit 0-7: **GPIO Output Selection**
  - 0x00: None
  - 0x02: GPIO1 Push-Pull, Active Low
  - 0x04: GPIO2 Push-Pull, Active Low
  - 0x20: GPIO5 Push-Pull, Active Low
  - 0x03: GPIO1 Active High
  - 0x05: GPIO2 Active High
  - 0x21: GPIO5 Active High
  - 0x0A: GPIO1 Open Drain
  - 0x0C: GPIO2 Open Drain
  - 0x28: GPIO5 Open Drain

Table A.11: General Channel Settings

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power				Normal Power				Reserved		Touch LTA	Prox LTA	Halt LTA	Res	Direc-tion	Dual

- Bit 12-15: **Low Power Beta Filter**
  - 4-bit value
- Bit 8-11: **Normal Power Beta Filter**
  - 4-bit value
- Bit 5: **Touch is LTA Dependent**
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Proximity is LTA Dependent**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Filter Halt is LTA Dependent**
  - 0: Disabled
  - 1: Enabled
- Bit 1: **Detection Direction**
  - 0: Detect in negative direction (Counts < LTA)
  - 1: Detect in positive direction (Counts > LTA)
- Bit 0: **Dual Directional Sensing**
  - 0: Dual directional sensing disabled
  - 1: Dual directional sensing enabled
  - Ignores Bit 1 when enabled

Table A.12: Filter Betas

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power Fast				Normal Power Fast				LTA Low Power				LTA Normal Power			

- Bit 12-15: **Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 8-11: **Normal Power Fast Beta Filter Value**
  - 4-bit value
- Bit 4-7: **LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Beta Filter Value**
  - 4-bit value

Table A.13: Conversion Frequency

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Period								Frequency Fraction							

- Bit 8-15: **Conversion Period**
  - $\frac{128}{FrequencyFraction} - 2$
  - Range: 0 - 127
- Bit 0-7: **Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 255

Table A.14: CRx Selection

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				RX3	RX2	RX1	RX0	Reserved						Reserved	

- Bit 11: **Rx3**
  - 0: Rx3 disabled
  - 1: Rx3 enabled

- Bit 10: **Rx2**
  - 0: Rx2 disabled
  - 1: Rx2 enabled
- Bit 9: **Rx1**
  - 0: Rx1 disabled
  - 1: Rx1 enabled
- Bit 8: **Rx0**
  - 0: Rx0 disabled
  - 1: Rx0 enabled

Table A.15: CTx Selection

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				GPIO4	GPIO3	GPIO0	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

- Bit 11: **GPIO4**
  - 0: GPIO4 disabled
  - 1: GPIO4 enabled
- Bit 10: **GPIO3**
  - 0: GPIO3 disabled
  - 1: GPIO3 enabled
- Bit 9: **GPIO0**
  - 0: GPIO0 disabled
  - 1: GPIO0 enabled
- Bit 8: **Tx8**
  - 0: Tx8 disabled
  - 1: Tx8 enabled
- Bit 7: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 6: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 5: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 4: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 3: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 2: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 1: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 0: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled

Table A.16: ATI Mode

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved													ATI Mode		

- Bit 0-2: **ATI Mode**
  - 000: Disabled
  - 001: Compensation only

- 010: From compensation Divider
- 011: From fine fractional divider
- 100: From course fractional divider
- 101: Full

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