IQS7222D DATASHEET

14 Channel Mutual / 8 Channel Self-capacitive Touch and Proximity Controller with I²C communications interface, configurable touch output pins and low power options

1 Device Overview

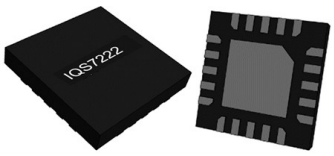
The IQS7222D ProxFusion® IC is a multi-sensor, multi-channel device mainly aimed at single finger trackpad applications. The device features I²C compatibility and on-chip computations that allow for an effective response even in the lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9x external sensor pad connections (QFN20)
- Configure up to 14 channels using the external connections [i]
- External sensor options:
  - Up to 8x self capacitive sensors
  - Up to 14x mutual capacitive sensors
  - Up to 4x inductive sensors
- Built-in basic functions:
  - Independent channel automatic tuning
  - Noise filtering
  - Debounce & Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Single finger gesture recognition:
    - Swipes (up, down, left, right)
    - Adjustable swipe length, angle and time duration
    - Taps (single taps)
    - Adjustable tap size and time duration
    - Flick
  - Trackpad:
    - XY coordinate slider output
    - Dynamic XY coordinate filtering
    - XY coordinate calibration
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY(up to fast plus -1MHz)
- Event and streaming modes
- Customizable user interface due to programmable memory
- Supply Voltage 1.8V to 3.5V
- Small packages
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4 mm pitch

RoHS2
Compliant

QFN20 package
Representation only



1.2 Applications

- Wearables
- Navigation controls
- Office equipment, toys, sanitary ware
- White goods and appliances
- Waterproof inductive buttons
- Low power wake-up / proximity sensor
- Replacement for electromechanical switches and keypads

1.3 Block Diagram

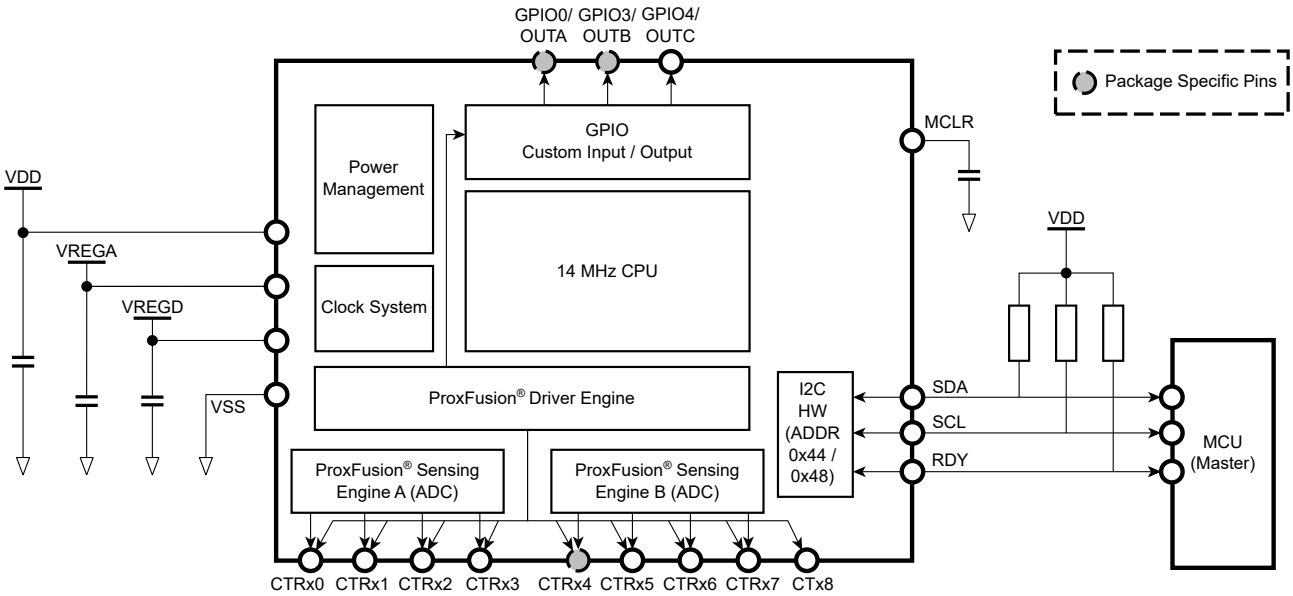


Figure 1.1: Functional Block Diagram[ii]

[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package

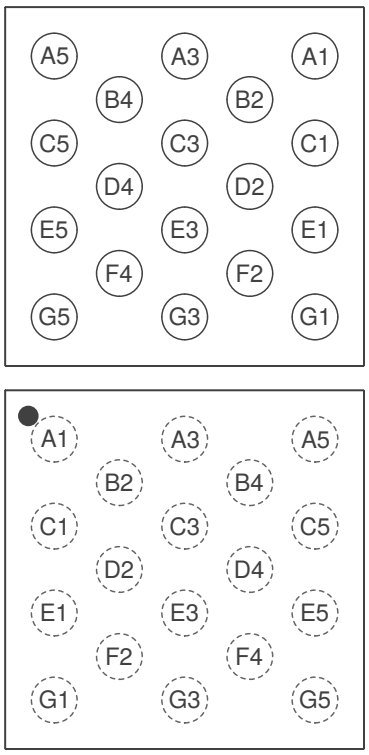
[ii] WLCSP18 packages do not have a CRx4 and combines GPIO0 and GPIO3

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

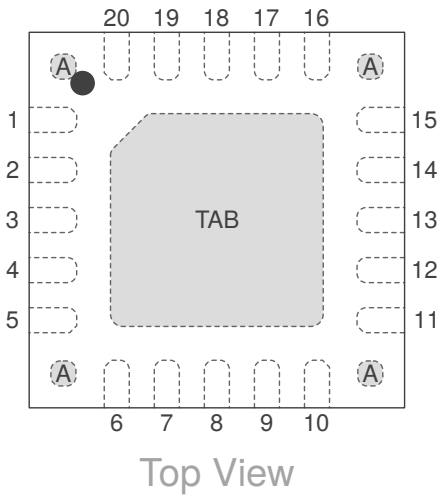
Table 2.1: 18-pin WLCSP18 Package



Pin no.	Signal
A1	OUTA/GPIO0/OUTB/GPIO3[i]
A3	SCL/GPIO2
A5	MCLR/GPIO6
B2	OUTC/GPIO4
B4	SDA/GPIO1
C1	CTx8/Vbias
C3	RDY/GPIO5
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8/Vbias
4	VREGA	14	OUTA/GPIO0
5	CRx0/CTx0	15	OUTB/GPIO3
6	CRx1/CTx1	16	OUTC/GPIO4
7	CRx2/CTx2	17	RDY/GPIO5
8	CRx3/CTx3	18	SCL/GPIO2
9	CRx4/CTx4	19	SDA/GPIO1
10	CRx5/CTx5	20	MCLR/GPIO6

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)

[i] Please note that OUTA/GPIO0 and OUTB/GPIO3 are connected together in the WLCSP18 package.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.
[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8/Vbias	Analog		VREGA
A1	14	OUTA/GPIO0	Digital		VDD
B4	19	SDA/GPIO1	Digital		VDD
A3	18	SCL/GPIO2	Digital		VDD
A1	15	OUTB/GPIO3	Digital		VDD
B2	16	OUTC/GPIO4	Digital		VDD
C3	17	RDY/GPIO5	Digital		VDD
A5	20	MCLR/GPIO6	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8/Vbias	C1	13	O	CTx8/Vbias pad
GPIO	OUTA/GPIO0	A1	14	O	OUTA/GPIO0 pad
	OUTB/GPIO3	A1	15	O	OUTB/GPIO3 pad
	OUTC/GPIO4	B2	16	O	OUTC/GPIO4 pad
	RDY/GPIO5	C3	17	O	RDY/GPIO5 pad
	MCLR/GPIO6	A5	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA/GPIO1	B4	19	IO	I^2C data
	SCL/GPIO2	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

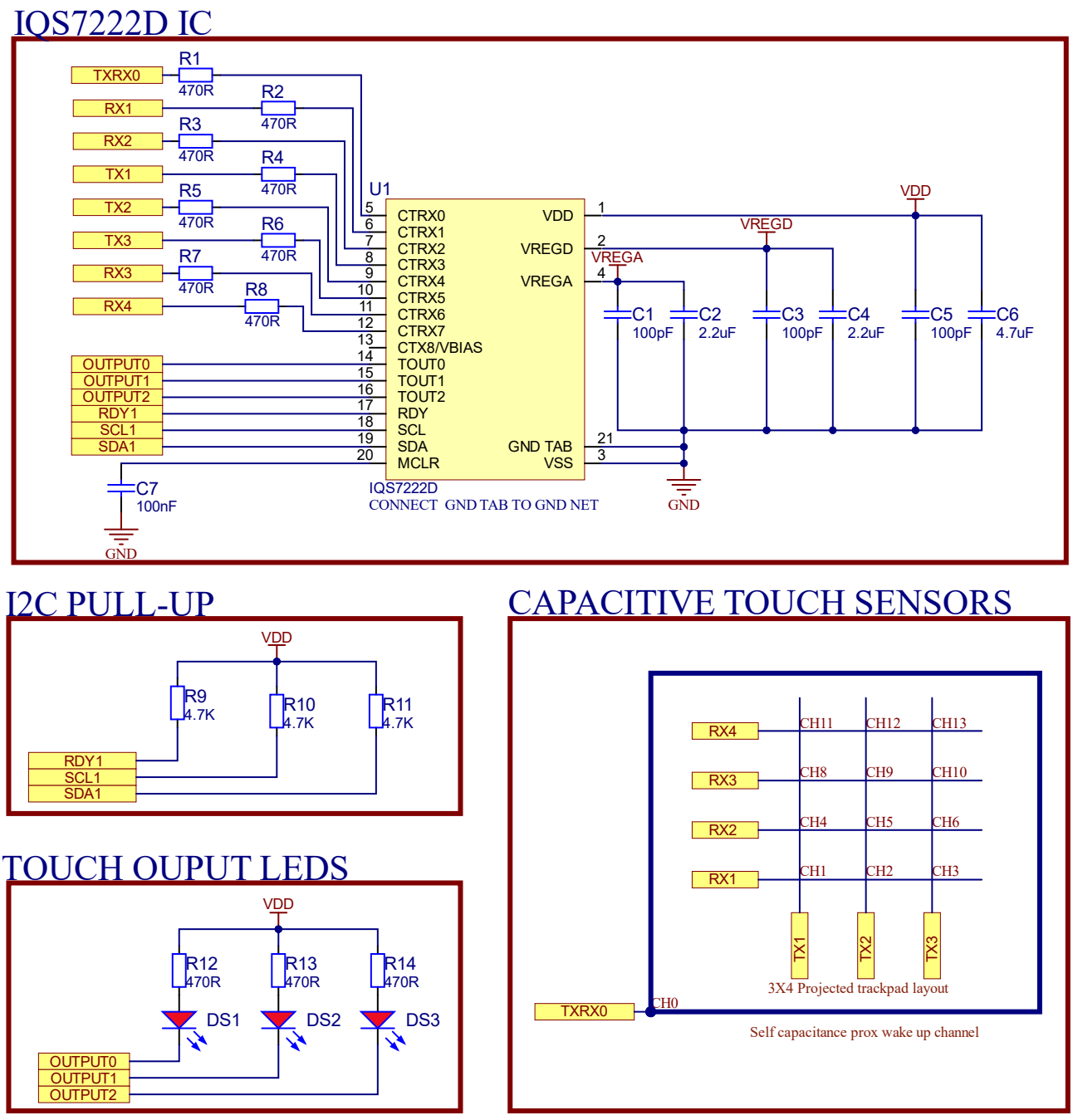


Figure 2.1: Wake-up and 3x4 Mutual Capacitive Trackpad Reference Schematic

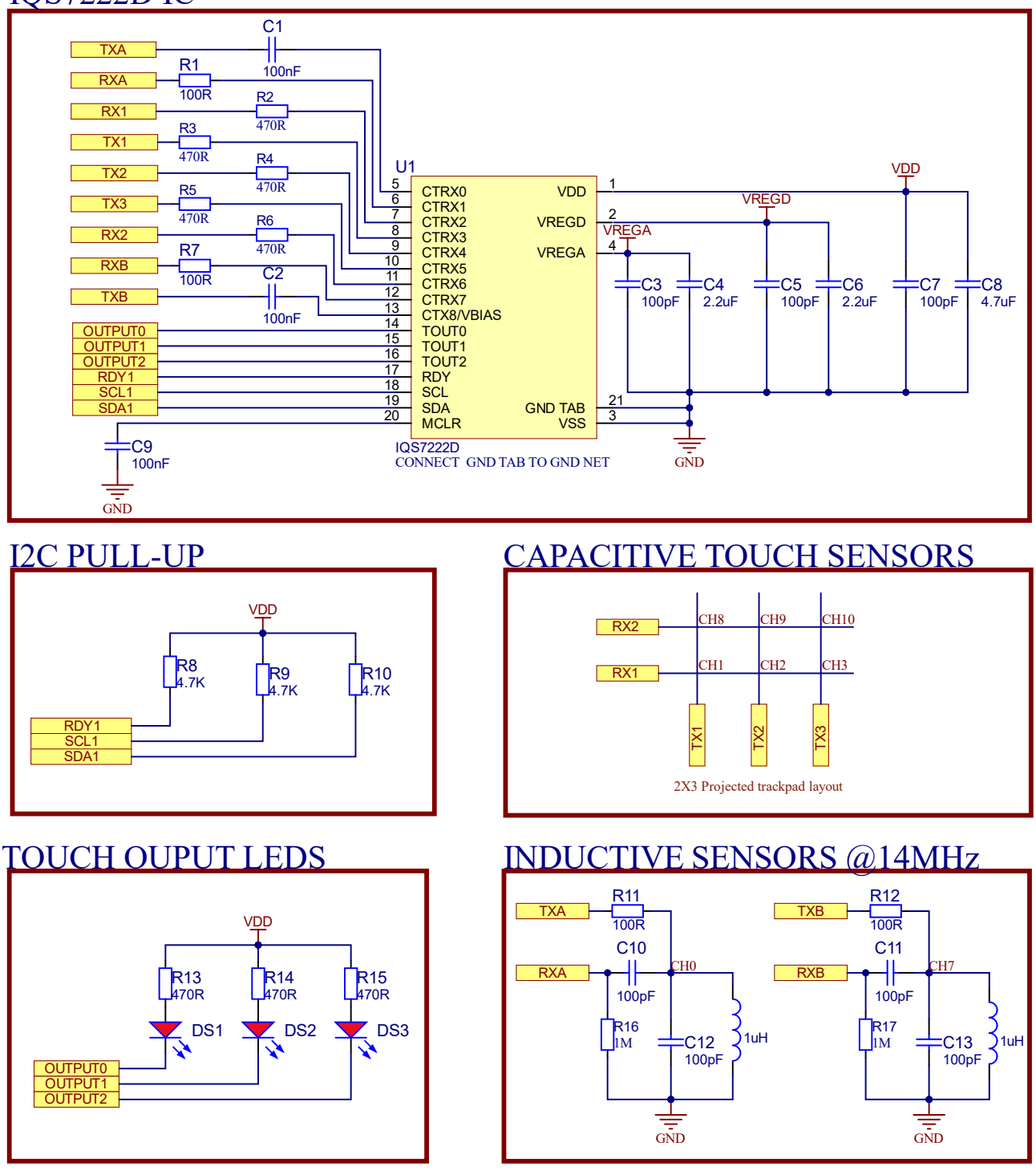


Figure 2.2: Inductive Buttons and 2x3 Mutual Capacitive Trackpad Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	2×C_{VREGA}	3×C_{VREGA}		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx–CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, F_{xfer} = 1 MHz Mutual-capacitance mode, F_{xfer} = 4 MHz			 100[ii] 25[ii]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
[ii] RCx = 0 Ω.

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Current Consumption

Mutual Inductive Mode Setup: ATI Target = 50, F_{OSC} = 14MHz
Self-Capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Mutual Capacitive Mode Setup: ATI Target = 512, F_{xfer} = 500kHz
Interface Selection: Event mode

Table 3.4: Typical Current Consumption for IQS7222D001

Power mode	Active channels	Report rate (Sampling rate) [ms]	Typical Current [µA]	
			1.8V	3.3V
Active Mode	Mutual Inductive (2 coils)	10		156
	Self-capacitive (10 channels)	16	365	367
	Mutual Capacitive slider and buttons	16	593	596
Idle	Mutual Inductive (2 coils)	80		20
	Self-capacitive (10 channels)	60	83	82
	Mutual Capacitive slider and buttons	60	114	115
ULP	Wake-up proximity - Distributed self channel	160	6.6	6.8
	Mutual Inductive (2 coils)	200		10

Mutual Capacitive Mode Setup: CH0/CH7 ATI Target = 800, CH1-6/CH8-13 ATI Target = 496, F_{xfer} = 1MHz
Interface Selection: Event mode

Table 3.5: Typical Current Consumption for IQS7222D102[vi]

Power mode	Active channels	Report rate (Sampling rate) [ms]	Typical Current [µA]	
			1.8V	3.3V
Active Mode	3x4 Mutual Capacitive trackpad (14 channels)	16	608	610
LP	3x4 Mutual Capacitive trackpad (14 channels)	60	158	159
ULP	3x4 Mutual Capacitive trackpad (14 channels)	150	14.6	14.9

[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.
[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[v] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times F_{xfer})}$ where C is the pin capacitance to VSS.
[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.
[vi] Please refer to product information notice PIN-230172 for more details

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

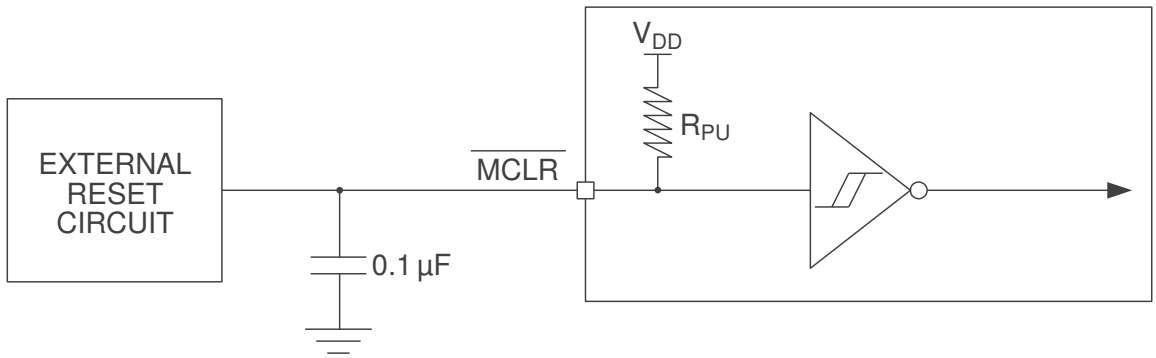


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

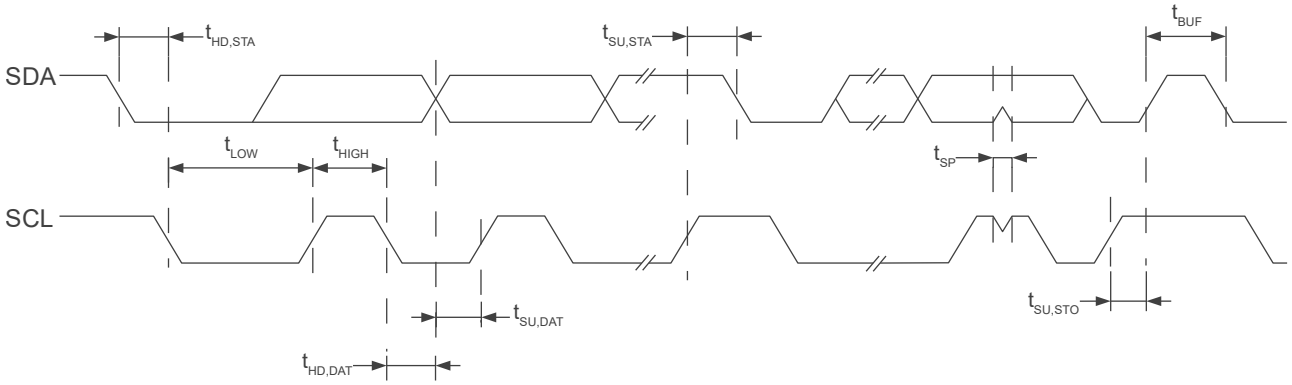


Figure 4.2: I²C Mode Timing Diagram

[i] Refers to OUTA, OUTB, OUTC, and RDY pins.

5 ProxFusion® Module

The IQS7222D contains dual ProxFusion® modules that uses patented technology to measure and process the sensor data. Two modules ensure a rapid response from multi-channel implementations. The multiple touch, proximity and weighted average (slider&wheel) outputs are the primary output from the sensor.

5.1 Channel Options

Self-capacitance, Mutual capacitance and Inductive designs are possible with the IQS7222D.

- Sensor pad design overview: AZD125
- Mutual capacitance button layout guide: AZD125
- Inductive design layout guide: AZD115

5.2 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

5.2.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *(Maximum counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.3.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xD0, bit3).

5.4 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductance, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please see contact Azoteq.

5.5 Automatic Re-ATI

5.5.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user

interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7222D, a status bit will set momentarily to indicate that this has occurred.

5.5.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.15.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{16}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and that the and the default boundary value is 1/16*800 = 50. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\textbf{Reference} > \textbf{850 or Reference} < \textbf{750}$$

The ATI algorithm executes in a short time, so goes unnoticed by the user.

5.5.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6 Sensing Modes

6.1 Power Mode and Mode Timeout

The IQS7222D offers 3 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption

In order to optimize power consumption and performance, power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time know as the "mode timeout". The value for the power mode to never timeout (i.e the current power mode will never progress to a lower power mode), is 0x00.

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitized raw input offers various damping options as defined in Table A.20 and Table A.21

Damping factor = Beta/256

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below, some are described, the other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

7.2.2 Software Reset

The IQS7222D can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 Automated Start-up

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up the device will automatically use the settings and perform the configuration/setup accordingly.

8.3 RF Immunity

The IQS7222D has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 2.2μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470Ω-1kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7222D supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7222D implements 8-bit addressing with 2 data bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The 7-bit device address for order code 001 is 0x44 (’01000100’) while the 7-bit device address for order code 102 is 0x48 (’01001000’). The full address byte for address 0x44 will thus be 0x89 (read) or 0x88 (write), and the full address byte for address 0x48 will be 0x91 (read) or 0x90 (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement 16-bit addressing scheme.

9.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to only address each Block as an 8-bit address, and then continue to clock into the next address locations. For example, if the procedure depicted below is followed, you will read the values from the hypothetical address 0xE000 to 0XE300:

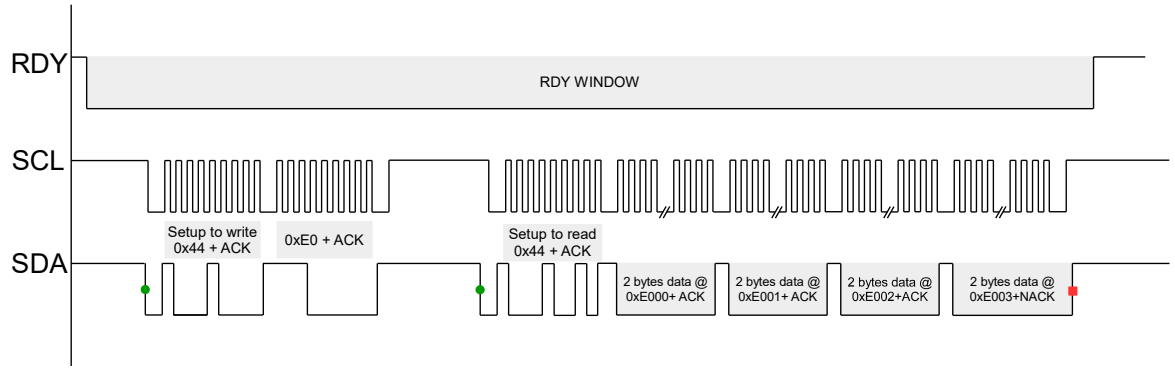


Figure 9.1: Extended 16-bit Addressing for Continuous Block

However, if you need to address a specific byte in that extended memory map space, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

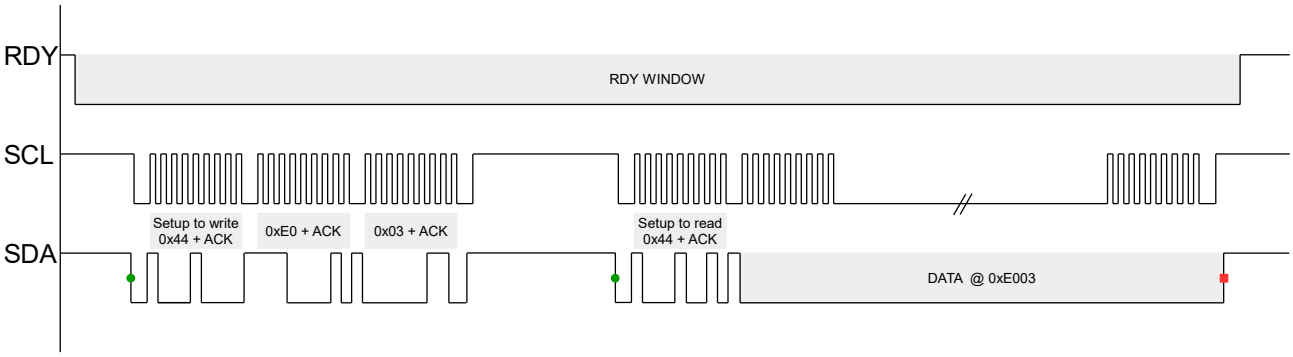


Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

The h file generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively -in a single block of data or the entire memory map, (refer to figure 9.1), or data can be written explicitly to a specific address (refer to figure 9.2). An example of the h file exported by the GUI and the order of the data, is shown in figure 9.3 below.

```
/* Change the Sensor 0 Settings */
/* Memory Map Position 0x30 - 0x39 */
#define SENSOR_0_SETUP_0          0x01
#define SENSOR_0_SETUP_1          0x07
```

Start address
LSB
MSB

Figure 9.3: Example of an H file Exported by the GUI

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive, however the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 500ms and can be adjusted in register 0xDC.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0xDA) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

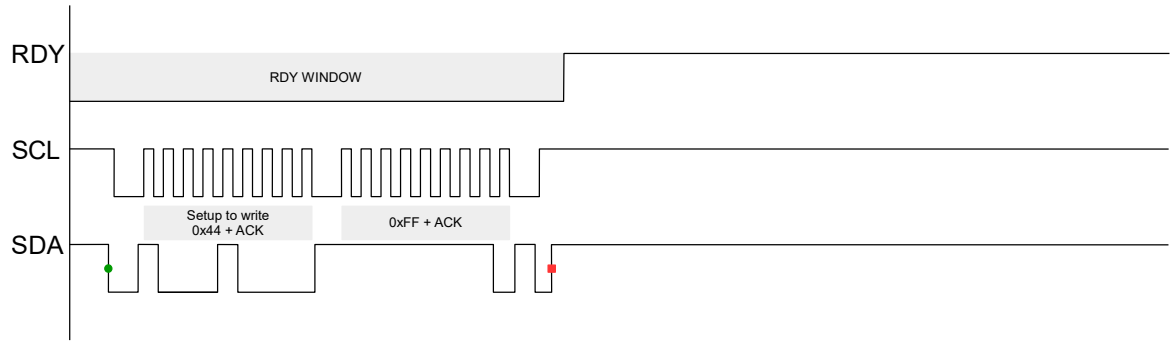


Figure 9.4: Force Stop Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

9.10 I²C Interface

The IQS7222D has 3 *I²C interface options*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0xD4* (normal power), register *0xD6* (low power) and register *0xD8* (ultra low power) respectively.

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.10.3 I²C Stream in Touch Mode

Stream in touch is a hybrid I²C mode between streaming mode and event mode. The device follows event mode I²C protocol but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I²C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

9.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *Events* register 0x11 to ensure all events flags are cleared otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode

9.11.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.3 and Table A.2:

- Power mode change
- Prox or touch event
- ATI error
- ATI active
- ATI Event

9.11.2 Force Communication

In streaming mode, the IQS7222D I²C will provide Ready (RDY) windows at intervals specified in the power mode report rate . Ideally, communication with the IQS7222D should only be initiated in a Ready window but a communication request described in figure 9.5 below, will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The time between the communication request and the opening of a RDY window (t_{wait}), is dependent on the report rate of the current power mode. t_{wait} can extend up to the current report rate +20% due to variability in the clock. Example, if a report rate of 100ms is chosen, the report rate may vary between 80ms and 120m[i].

There is a possibility of a communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period. However, it is essential to retry at different timings that are

[i] Please contact Azoteq for an application specific value of t_{wait}

not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional precautionary measure, the IC can be reset using the MCLR pin and reinitialized if there is no response after a specified number of retries.

A force communication request should be avoided while RDY is in the LOW state. If a communication request is sent at the exact moment when an event causes RDY to go low, the window will close again after sending the I^2C STOP signal. In such a scenario, the device will provide an invalid communication response (0xEE) because the host is attempting to read from the device outside of a communication window (i.e. while RDY is high). To prevent this issue, it is recommended to read the product number during each ready window to ensure that the response received is valid.

A slight delay may occur in receiving an acknowledgement (ACK) when attempting force communication while the device is in an internal lower power mode with certain peripherals switched off. This delay can occur regardless of the state of the current system power mode.

The communication request sequence is shown in figure 9.5 below.

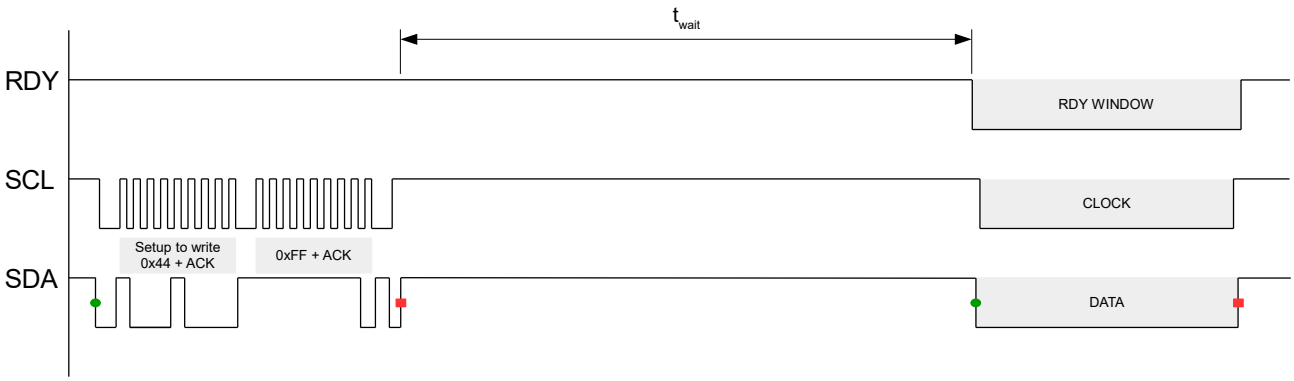


Figure 9.5: Force Communication Sequence

9.12 Program Flow Diagram

The program flow for event mode communication is shown in 9.6

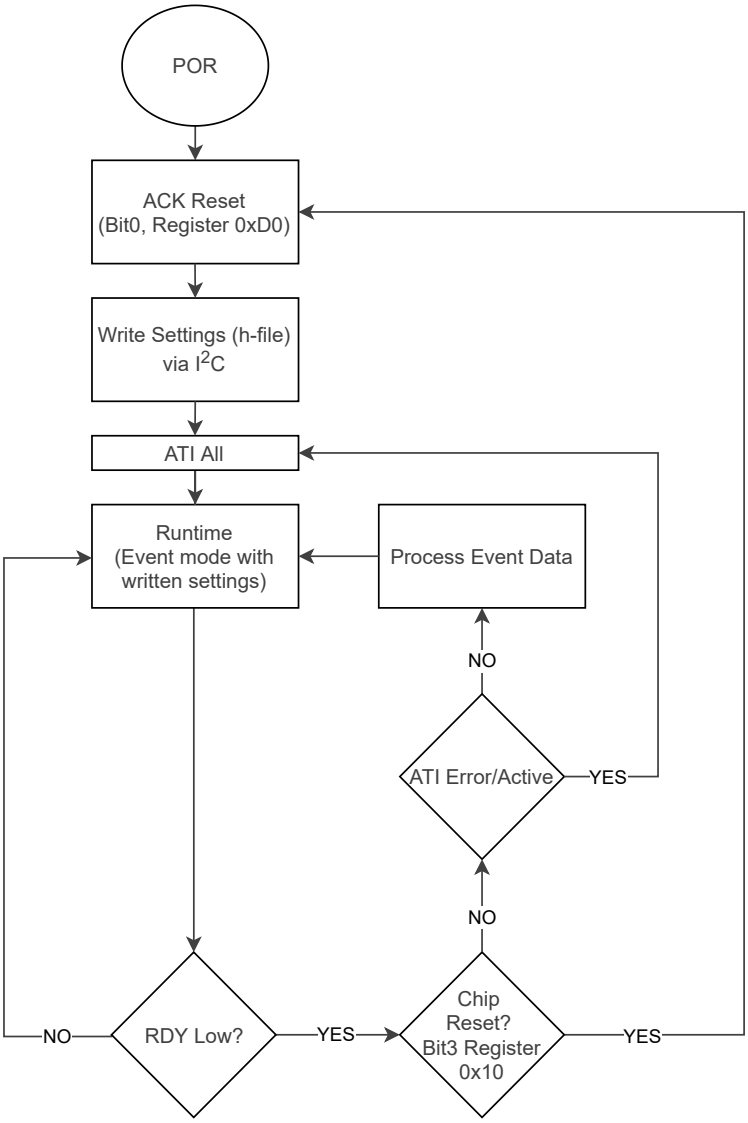


Figure 9.6: Program Flow Diagram

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only	**Device Status**	
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Prox event States	See Table A.4
0x13	Touch event States	See Table A.5
0x14	Trackpad X Output	16-bit value
0x15	Trackpad Y Output	
0x16	Trackpad Event Flags	See Table A.6
Read Only	**Channel Counts**	
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
0x28	Channel 8 Counts	
0x29	Channel 9 Counts	
0x2A	Channel 10 Counts	
0x2B	Channel 11 Counts	
0x2C	Channel 12 Counts	
0x2D	Channel 13 Counts	
Read-Write	**Channel LTA**	
0x30	Channel 0 LTA	16-bit value
0x31	Channel 1 LTA	
0x32	Channel 2 LTA	
0x33	Channel 3 LTA	
0x34	Channel 4 LTA	
0x35	Channel 5 LTA	
0x36	Channel 6 LTA	
0x37	Channel 7 LTA	
0x38	Channel 8 LTA	
0x39	Channel 9 LTA	
0x3A	Channel 10 LTA	
0x3B	Channel 11 LTA	
0x3C	Channel 12 LTA	
0x3D	Channel 13 LTA	
Read-Write	**Cycle Setup**	
0x8000	Cycle Setup 0	See Table A.7
0x8001		See Table A.8
0x8100	Cycle Setup 1	See Table A.7
0x8101		See Table A.8
0x8200	Cycle Setup 2	See Table A.7
0x8201		See Table A.8
0x8300	Cycle Setup 3	See Table A.7
0x8301		See Table A.8

0x8400	Cycle Setup 4	See Table A.7
0x8401		See Table A.8
0x8500	Cycle Setup 5	See Table A.7
0x8501		See Table A.8
0x8600	Cycle Setup 6	See Table A.7
0x8601		See Table A.8
0x8700	Global Cycle Setup	See Table A.9
0x8701	Coarse and Fine Multiplier Preloads	See Table A.10
0x8702	Compensation Preload	See Table A.11
Read-Write	**Button Setup - Thresholds, Hysteresis and Debounce**	
0x9000	Button Setup 0	See Table A.12
0x9001		See Table A.13
0x9002		See Table A.14
0x9100	Button Setup 1	See Table A.12
0x9101		See Table A.13
0x9102		See Table A.14
0x9200	Button Setup 2	See Table A.12
0x9201		See Table A.13
0x9202		See Table A.14
0x9300	Button Setup 3	See Table A.12
0x9301		See Table A.13
0x9302		See Table A.14
0x9400	Button Setup 4	See Table A.12
0x9401		See Table A.13
0x9402		See Table A.14
0x9500	Button Setup 5	See Table A.12
0x9501		See Table A.13
0x9502		See Table A.14
0x9600	Button Setup 6	See Table A.12
0x9601		See Table A.13
0x9602		See Table A.14
0x9700	Button Setup 7	See Table A.12
0x9701		See Table A.13
0x9702		See Table A.14
0x9800	Button Setup 8	See Table A.12
0x9801		See Table A.13
0x9802		See Table A.14
0x9900	Button Setup 9	See Table A.12
0x9901		See Table A.13
0x9902		See Table A.14
0x9A00	Button Setup 10	See Table A.12
0x9A01		See Table A.13
0x9A02		See Table A.14
0x9B00	Button Setup 11	See Table A.12
0x9B01		See Table A.13
0x9B02		See Table A.14
0x9C00	Button Setup 12	See Table A.12
0x9C01		See Table A.13
0x9C02		See Table A.14
0x9D00	Button Setup 13	See Table A.12
0x9D01		See Table A.13
0x9D02		See Table A.14

	Channel Setup- ATI Parameters and Rx Select	
Read-Write	**Channel 0**	
0xA000	CRX Select and General Channel Setup	See Table A.15
0xA001	ATI Base and Target	See Table A.17
0xA002	Fine and Coarse Multipliers	See Table A.18
0xA003	ATI Compensation	See Table A.19
Read-Write	**Channel 1**	
0xA100	CRX Select and General Channel Setup	See Table A.15
0xA101	ATI Base and Target	See Table A.17
0xA102	Fine and Coarse Multipliers	See Table A.18
0xA103	ATI Compensation	See Table A.19
Read-Write	**Channel 2**	
0xA200	CRX Select and General Channel Setup	See Table A.15
0xA201	ATI Base and Target	See Table A.17
0xA202	Fine and Coarse Multipliers	See Table A.18
0xA203	ATI Compensation	See Table A.19
Read-Write	**Channel 3**	
0xA300	CRX Select and General Channel Setup	See Table A.15
0xA301	ATI Base and Target	See Table A.17
0xA302	Fine and Coarse Multipliers	See Table A.18
0xA303	ATI Compensation	See Table A.19
Read-Write	**Channel 4**	
0xA400	CRX Select and General Channel Setup	See Table A.15
0xA401	ATI Base and Target	See Table A.17
0xA402	Fine and Coarse Multipliers	See Table A.18
0xA403	ATI Compensation	See Table A.19
Read-Write	**Channel 5**	
0xA500	CRX Select and General Channel Setup	See Table A.16
0xA501	ATI Base and Target	See Table A.17
0xA502	Fine and Coarse Multipliers	See Table A.18
0xA503	ATI Compensation	See Table A.19
Read-Write	**Channel 6**	
0xA600	CRX Select and General Channel Setup	See Table A.16
0xA601	ATI Base and Target	See Table A.17
0xA602	Fine and Coarse Multipliers	See Table A.18
0xA603	ATI Compensation	See Table A.19
Read-Write	**Channel 7**	
0xA700	CRX Select and General Channel Setup	See Table A.16
0xA701	ATI Base and Target	See Table A.17
0xA702	Fine and Coarse Multipliers	See Table A.18
0xA703	ATI Compensation	See Table A.19
Read-Write	**Channel 8**	
0xA800	CRX Select and General Channel Setup	See Table A.16
0xA801	ATI Base and Target	See Table A.17
0xA802	Fine and Coarse Multipliers	See Table A.18
0xA803	ATI Compensation	See Table A.19
Read-Write	**Channel 9**	
0xA900	CRX Select and General Channel Setup	See Table A.16
0xA901	ATI Base and Target	See Table A.17
0xA902	Fine and Coarse Multipliers	See Table A.18
0xA903	ATI Compensation	See Table A.19

Read-Write	Channel 10	
0xAA00	CRX Select and General Channel Setup	See Table A.16
0xAA01	ATI Base and Target	See Table A.17
0xAA02	Fine and Coarse Multipliers	See Table A.18
0xAA03	ATI Compensation	See Table A.19
Read-Write	**Channel 11**	
0xAB00	CRX Select and General Channel Setup	See Table A.16
0xAB01	ATI Base and Target	See Table A.17
0xAB02	Fine and Coarse Multipliers	See Table A.18
0xAB03	ATI Compensation	See Table A.19
Read-Write	**Channel 12**	
0xAC00	CRX Select and General Channel Setup	See Table A.16
0xAC01	ATI Base and Target	See Table A.17
0xAC02	Fine and Coarse Multipliers	See Table A.18
0xAC03	ATI Compensation	See Table A.19
Read-Write	**Channel 13**	
0xAD00	CRX Select and General Channel Setup	See Table A.16
0xAD01	ATI Base and Target	See Table A.17
0xAD02	Fine and Coarse Multipliers	See Table A.18
0xAD03	ATI Compensation	See Table A.19
Read-Write	**Filter Betas**	
0xAE00	Filter Beta	See Table A.20
0xAE01	Fast Filter Beta	See Table A.21
Read-Write	**Trackpad Setup**	
0xB000	Trackpad General Setup	See Table A.22
0xB001	X and Y Lower Calibration	See Table A.23
0xB002	X and Y Upper Calibration	See Table A.24
0xB003	Top and Bottom Speed	See Table A.25
0xB004	X Resolution	16-bit value
0xB005	Y Resolution	
0xB006	Channel Enable Mask	See Table A.26
0xB007	Enable Status Link	See Table A.27
Read-Write	**Trackpad Delta Links**	
0xB008	Delta Link 0	See Table A.28
0xB009	Delta Link 1	
0xB00A	Delta Link 2	
0xB00B	Delta Link 3	
0xB00C	Delta Link 4	
0xB00D	Delta Link 5	
0xB00E	Delta Link 6	
0xB00F	Delta Link 7	
0xB010	Delta Link 8	
0xB011	Delta Link 9	
0xB012	Delta Link 10	
0xB013	Delta Link 11	
Read-Write	**Trackpad Gestures**	
0xB014	Trackpad Gestures 0	See Table A.29
0xB015	Trackpad Gestures 1	See Table A.30
0xB016	Tap Distance	See Table A.31
0xB017	Swipe Distance	See Table A.32
Read-Write	**Output Port Pin Settings**	

0xC000	Output Port 0 Enable and Configuration Settings	See Table A.33
0xC001	Output Port 0 Channel Mask	See Table A.34
0xC002	Output Port 0 Enable Status Link	See Table A.35
0xC100	Output Port 1 Enable and Configuration Settings	See Table A.33
0xC101	Output Port 1 Channel Mask	See Table A.34
0xC102	Output Port 1 Enable Status Link	See Table A.35
0xC200	Output Port 2 Enable and Configuration Settings	See Table A.33
0xC201	Output Port 2 Channel Mask	See Table A.34
0xC202	Output Port 2 Enable Status Link	See Table A.35
Read-Write	**PMU and System Settings**	
0xD0	Control settings	See Table A.36
0xD1	ATI Error Timeout	16-bit value * 500ms
0xD2	ATI Report Rate	16-bit value (ms)
0xD3	Normal Power Mode Timeout	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xD5	Low Power Mode Timeout	16-bit value (ms)
0xD6	Low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xD7	Normal Power Update rate in Ultra-low Power Mode	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3276
0xD9	ULP Entry Mask	See table A.37
0xDA	Event Enable	See Table A.38
0xDB	I^2C Communication	See Table A.39
0xDC	Output port Override	See Table A.40
0xDD	I^2C Communications Timeout	See Table A.41

11 Implementation and Layout

11.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

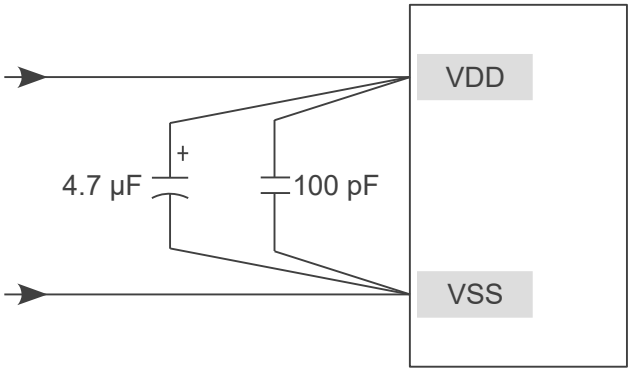


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 11.2 below shows an example placement of the VREG capacitors.

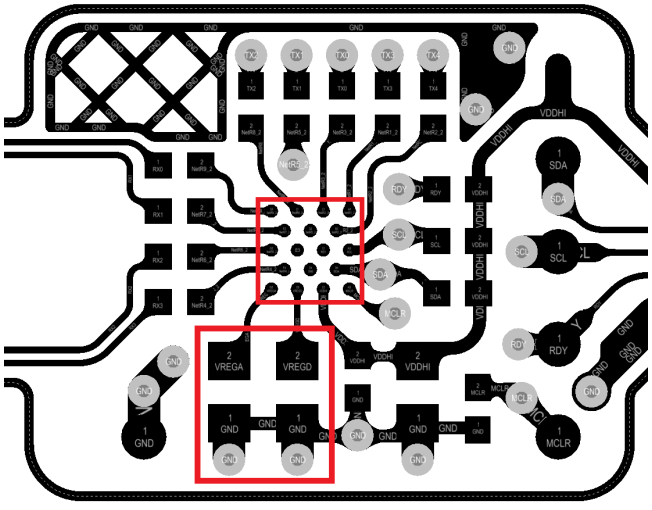


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

12 Ordering Information

12.1 Ordering Code

IQS7222D zzz ppb

IC NAME				IQS7222D
CONFIGURATION	zzz	=	001	I^2C address = 0x44
		=	102	I^2C address = 0x48[i]
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QF	QFN-20 package
		=	QN	QFN-20 package (On special order only[ii])
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Figure 12.1: Order Code Description

12.2 Top Marking

12.2.1 WLCSP18 Package

Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 1

Product Name
ppp = product code
xx = batchcode

12.2.3 QFN20 Package Marking Option 2

Product Name
ppp = product code
xx = batchcode

[i] Please refer to product information notice PIN-230172 for more details
[ii] Special order codes are subject to larger minimum order quantities, longer lead times and are non-cancelable, non-returnable.

13 Package Specification

13.1 Package Outline Description – WLCSP18

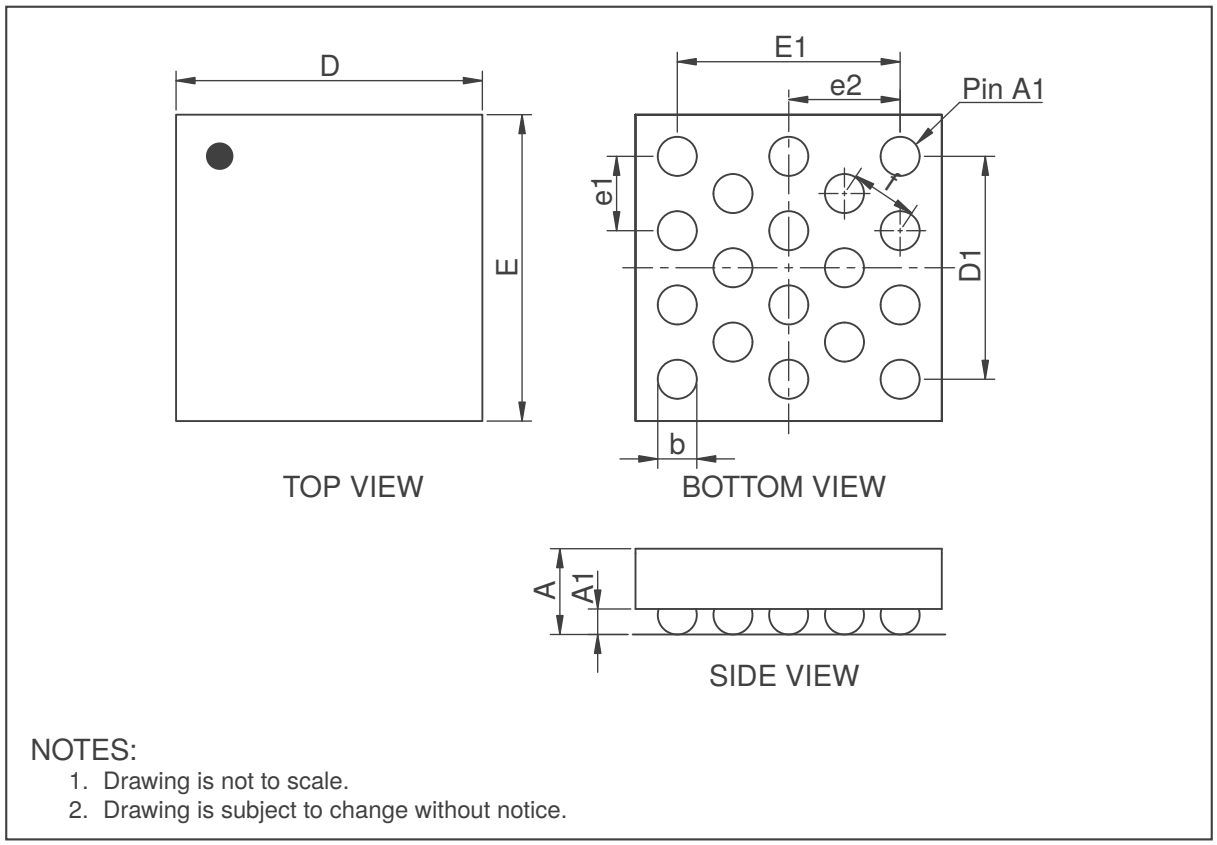
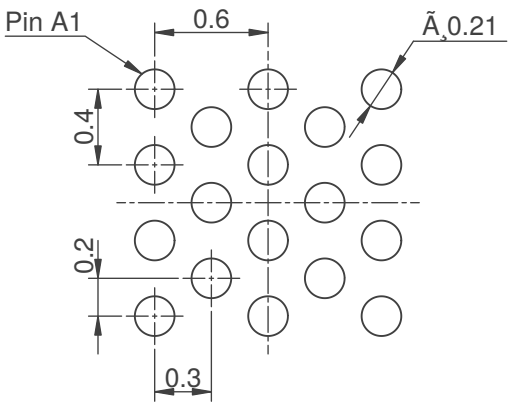


Figure 13.1: WLCSP (1.62x1.62)-18 Package Outline Visual Description

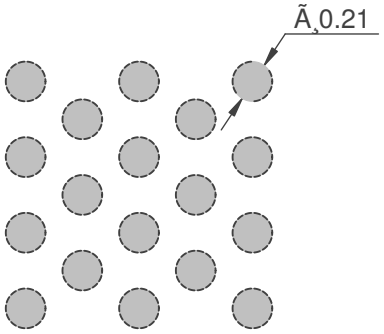
Table 13.1: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1	1.200 BSC		
E1	1.200 BSC		
e1	0.400 BSC		
e2	0.600 BSC		
f	0.360 REF		

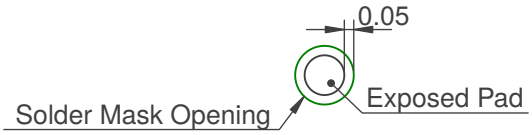
13.2 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: WLCSP18 Recommended Footprint

13.3 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

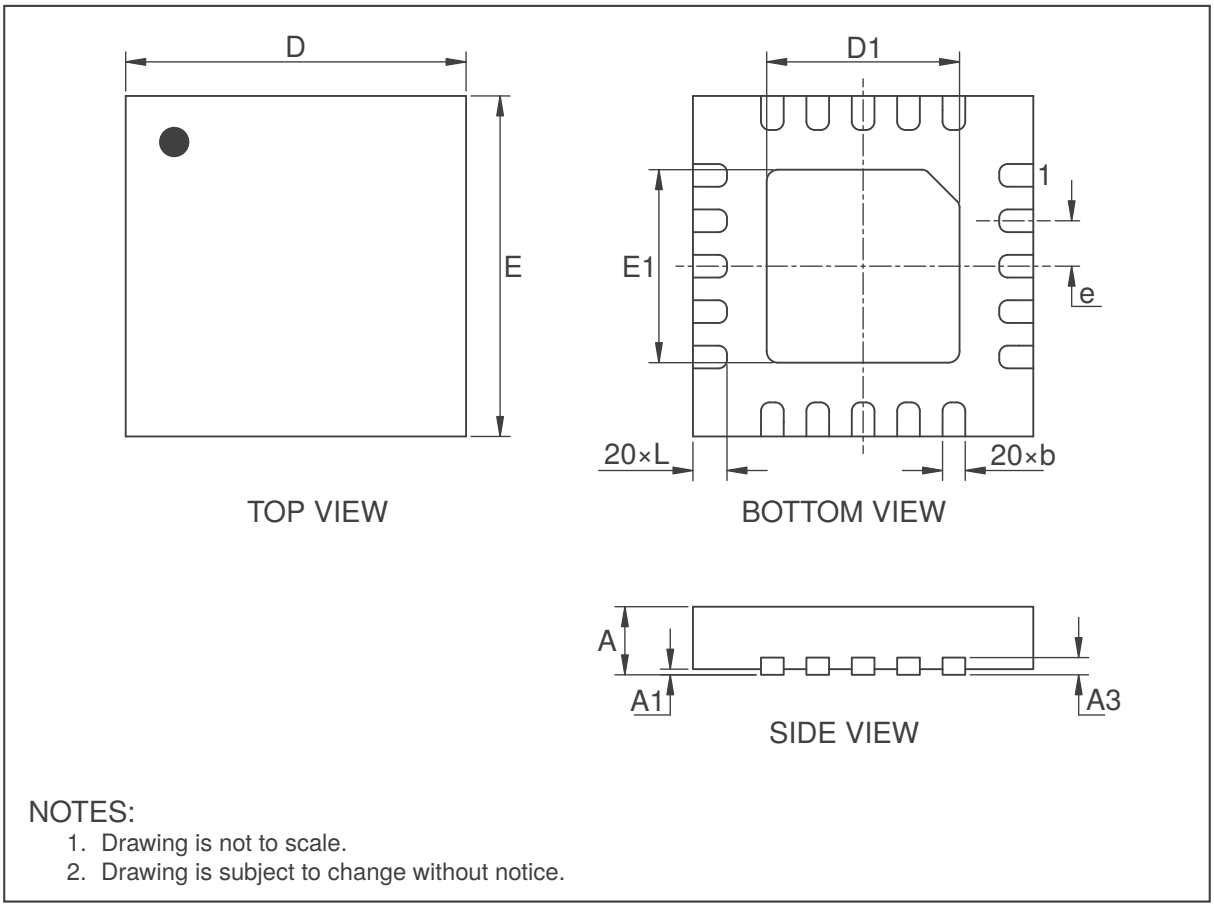
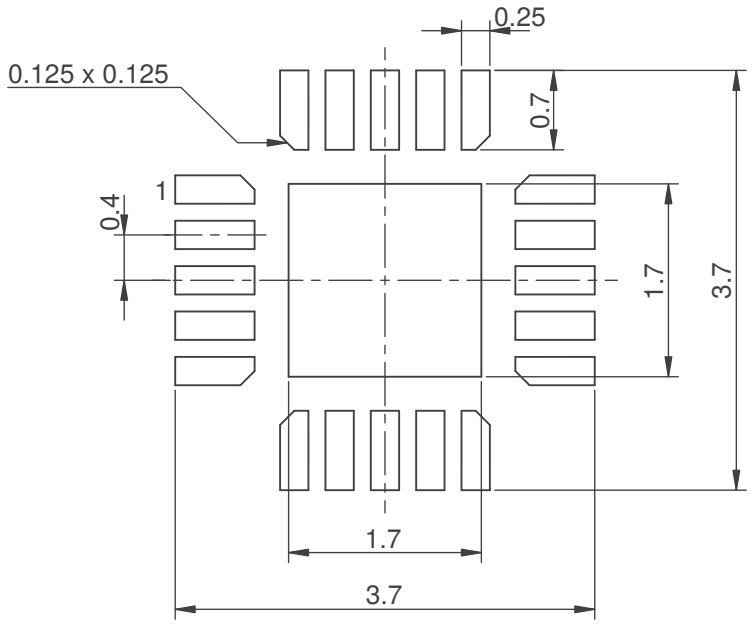


Figure 13.3: QFN (3x3)-20 (QFR) Package Outline Visual Description

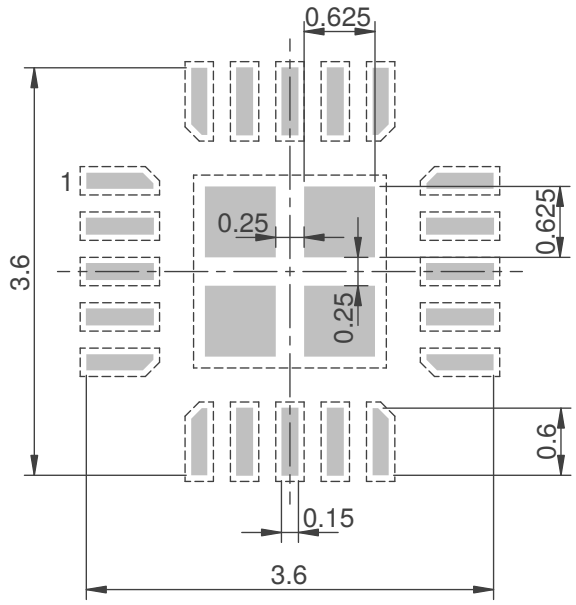
Table 13.2: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

13.4 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.4: QFN (3x3)-20 (QFR) Recommended Footprint

13.5 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

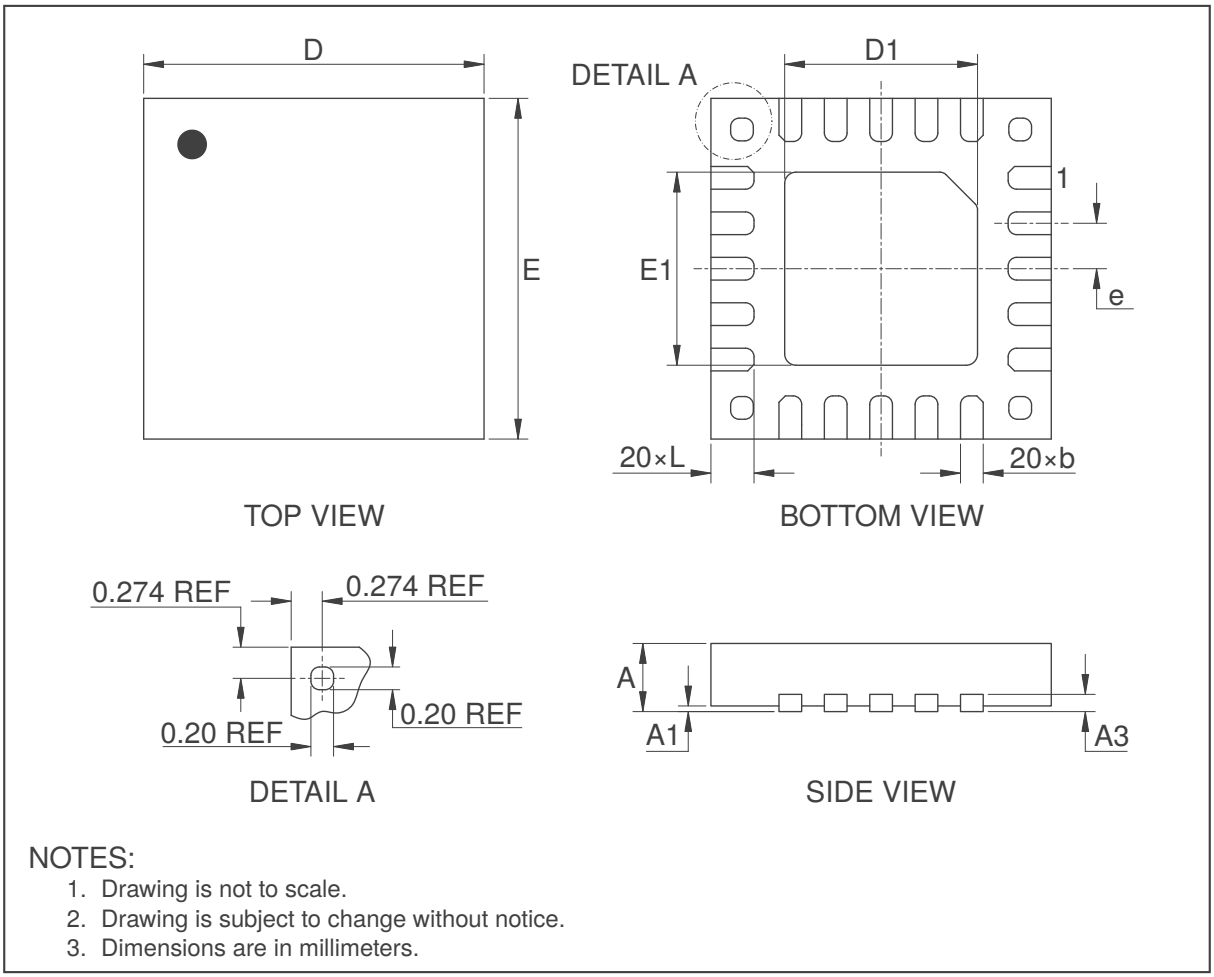
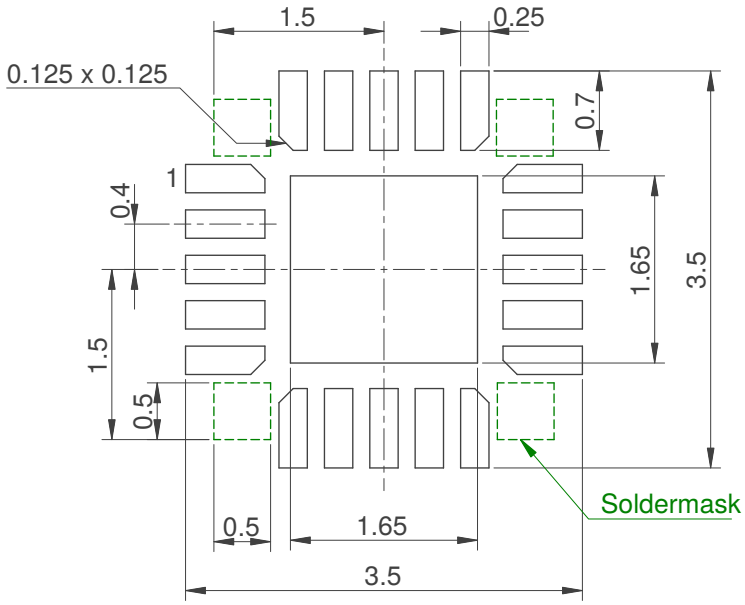


Figure 13.5: QFN (3x3)-20 (QNR) Package Outline Visual Description

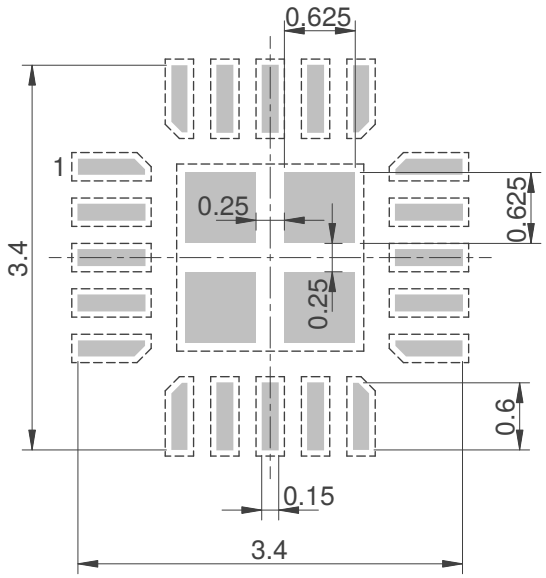
Table 13.3: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

13.6 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



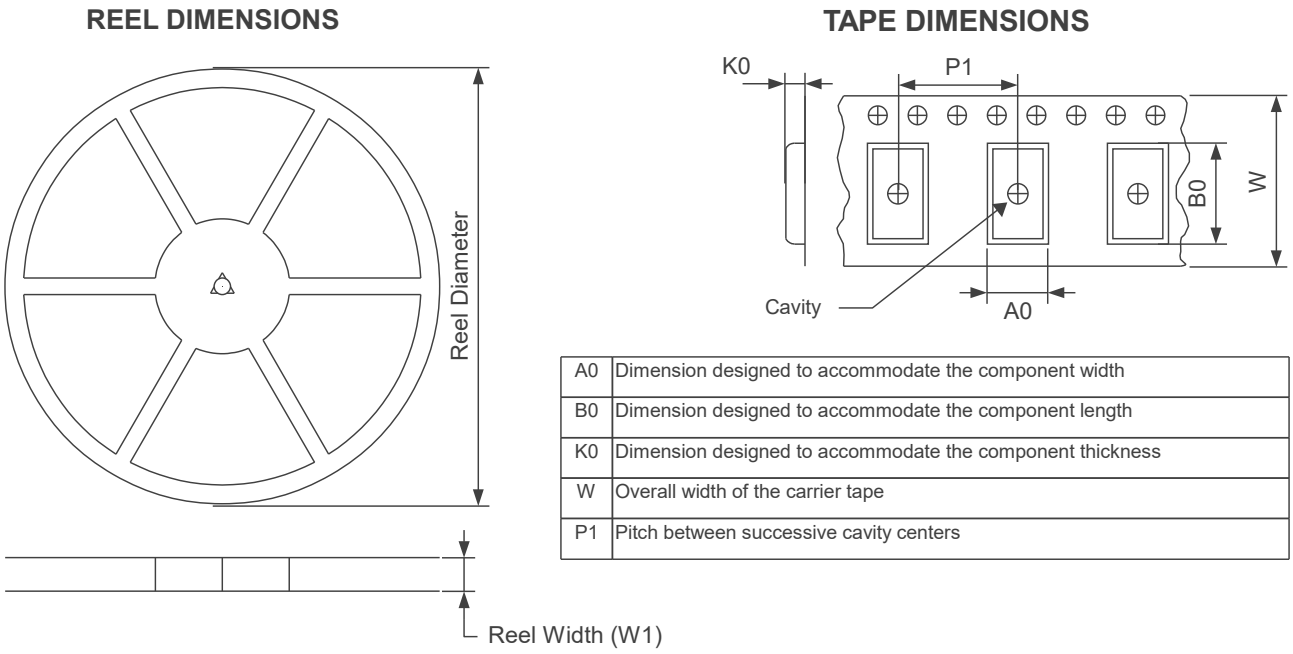
RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 13.6: QFN (3x3)-20 (QNR) Recommended Footprint

13.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 13.7: Tape and Reel Specification

Table 13.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

13.8 Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Please note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value	Order Code	
0x00	Application Version Info	Product Number	1046		16-bit value
0x01		Major Version	1		
0x02		Minor Version	1	001	
			2	102[i]	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP update	Power mode		Reset	Res	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 6: **NP Update**
  - 0: No Normal Power Update occurred
  - 1: Normal Power update occurred
- Bit 4-5: **Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Res	Track-pad	Reserved								Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 10: **Trackpad Event**

[i] Please refer to product information notice PIN-230172 for more details

- 0: No Trackpad Event occurred
- 1: Trackpad Event occurred

› Bit 1: **Touch Event**
- 0: No Touch Event occurred
- 1: Touch Event occurred

› Bit 0: **Prox Event**
- 0: No Prox Event occurred
- 1: Prox Event occurred

Table A.4: Proximity Event States

Register: 0x12

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

› Bit 0-13: **Channel Prox Event**
- 0: No prox event occurred on channel
- 1: Prox event occurred on channel

Table A.5: Touch Event States

Register: 0x13

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

› Bit 0-13: **Channel Touch Event**
- 0: No touch event occurred on channel
- 1: Touch event occurred on channel

Table A.6: Trackpad Event Flags

Register: 0x16

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved										Swipe Y -	Swipe X -	Swipe Y	Swipe X	Flick	Tap

› Bit 5: **Swipe Y Negative**
- 0: Positive Swipe in Y direction
- 1: Negative Swipe in Y direction

› Bit 4: **Swipe X Negative**
- 0: Positive Swipe in X direction
- 1: Negative Swipe in X direction

› Bit 3: **Swipe Y**
- 0: No Swipe in Y direction
- 1: Swipe in Y direction

› Bit 2: **Swipe X**
- 0: No Swipe in X direction
- 1: Swipe in X direction

› Bit 1: **Flick**
- 0: No flick event occurred
- 1: Flick event occurred

› Bit 0: **Tap**
- 0: No tap event occurred
- 1: Tap event occurred

Table A.7: Cycle Setup 0

Register: 0x8000, 0x8100, 0x8200, 0x8300, 0x8400, 0x8500, 0x8600

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - The calculation of the charge transfer frequency (f_{xfer} is shown below. The relevant formula is determined by the value of the dead time enabled bit (refer to table A.8)
  - Dead time disabled: $f_{xfer} = \frac{f_clk}{2*period+2}$
  - Dead time enabled: $f_{xfer} = \frac{f_clk}{2*period+3}$
  - Range: 0 - 127
- Bit 0-7: **Conversion Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 255
- Note: if Conversion frequency fraction is fixed at 127 and dead time is enabled, the following values of the conversion period will result in the corresponding charge transfer frequencies:
  - 1: 2MHz
  - 5: 1MHz[ii]
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

Table A.8: Cycle Setup 1

Register: 0x8001, 0x8101, 0x8201, 0x8301, 0x8401, 0x8501, 0x8601

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Inactive Rx - GND	Dead time en- abled	FOSC TX Freq	VBIAS En- able	PXS Mode		

- Bit 15: **Tx8**
  - 0: Tx8 disabled
  - 1: Tx8 enabled
- Bit 14: **Tx7**
  - 0: Tx7 disabled
  - 1: Tx7 enabled
- Bit 13: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 12: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 11: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 10: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 9: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 8: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 7: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled
- Bit 6: **Inactive Rx GND**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - 0: Dead-time disabled
  - 1: Dead-time enabled
- Bit 4: **TX FOSC Frequency**

[ii] Please note: The maximum charge transfer frequency for mutual capacitive mode (refer to table A.8) is 1MHz

- 0: Disabled
- 1: Enabled

› Bit 3: **VBIAS Enabled**
- 0: VBIAS disabled
- 1: VBIAS enabled

› Bit 0-2: **PXS Mode**
- 000: None
- 001: Self-capacitive
- 010: Mutual capacitive
- 011: Mutual inductance

Table A.9: Global Cycle Setup

Register: 0x8700

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Maximum counts		0	1	0	1	1	1	1	0	0	Auto Mode		1	1

› Bit 13-14: **Maximum counts**
- 00: 1023
- 01: 2047
- 10: 4095
- 11: 16384

› Bit 2-3: **Auto Mode**
- Number of conversions created before each interrupt is generated
- 00: 4
- 01: 8
- 10: 16
- 11: 32

Table A.10: Coarse and Fine Multipliers Preload

Register: 0x8701

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Multiplier Preload					Reserved				Coarse Multiplier Preload				

› Bit 0-4: **Coarse Multiplier Preload**
- 5-bit coarse multiplier preload value

› Bit 9-13: **Fine Multiplier Preload**
- 5-bit fine multiplier preload value

Table A.11: ATI Compensation Preload

Register: 0x8702

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

› Bit 0-9: **ATI Compensation Preload**
- 10-bit preload value

Table A.12: Button Setup 0

Register: 0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900, 0x9A00, 0x9B00, 0x9C00, 0x9D00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				0	Proximity Threshold						

› Bit 12-15: **Exit Debounce Value**
- 0000: Debounce disabled
- 4-bit value

› Bit 8-11: **Enter Debounce Value**
- 0000: Debounce disabled
- 4-bit value

› Bit 0-6: **Proximity Threshold**
- 7-bit value

Table A.13: Button Setup 1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901, 0x9A01, 0x9B01, 0x9C01, 0x9D01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{LTA}{256}$*Threshold bit value - $\frac{LTA}{2^16}$*Hysteresis bit value
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * 8\text{bit value}$

Table A.14: Button Setup 2

Register: 0x9002, 0x9102, 0x9202, 0x9302, 0x9402, 0x9502, 0x9602, 0x9702, 0x9802, 0x9902, 0x9A02, 0x9B02, 0x9C02, 0x9D02

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout								Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - 8-bit value * 500ms
  - 0: Never timeout
- Bit 0-7: **Prox Event Timeout**
  - 8-bit value * 500ms
  - 0: Never timeout

Table A.15: CRX Select and General Channel Setup(CH0-CH6)

Register: 0xA000, 0xA100, 0xA200, 0xA300, 0xA400, 0xA500, 0xA600

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Res	Filter En	ATI Band		Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs 80pF	0v5 Rev	Proj Bias Select	

- Bit 14: **AC Filter Enable**
  - 0: AC Filter disabled
  - 1: AC Filter enabled
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled

- Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **VBIAS enabled**
  - 0: VBIAS disabled
  - 1: VBIAS enabled
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.16: CRX Select and General Channel Setup(CH7-CH13)

Register: 0xA700, 0xA800, 0xA900, 0xAA00, 0xAB00, 0xAC00, 0xAD00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Res	Filter En	ATI Band		Global halt	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs 80pF	0v5 Rev	Proj Bias Select	

- Bit 14: **AC Filter Enable**
  - 0: AC Filter disabled
  - 1: AC Filter enabled
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
- Bit 6: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled
- Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
- Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
- Bit 3: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **VBIAS enabled**
  - 0: VBIAS disabled
  - 1: VBIAS enabled
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA

- 10: 7μA
- 11: 10μA

Table A.17: ATI Base and Target

Register: 0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601, 0xA701, 0xA801, 0xA901, 0xAA01, 0xAB01, 0xAC01, 0xAD01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.18: Fine and Coarse Multipliers

Register: 0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602, 0xA702, 0xA802, 0xA902, 0xAA02, 0xAB02, 0xAC02, 0xAD02

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.19: ATI Compensation

Register: 0xA003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603, 0xA703, 0xA803, 0xA903, 0xAA03, 0xAB03, 0xAC03, 0xAD03

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.20: Filter Betas

Register: 0xAE00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

- Bit 12-15: **LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 8-11: **LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.21: Fast Filter Betas

Register: 0xAE01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 4-7: **LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.22: Trackpad General Setup

Register: 0xB000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				Static Filter Enable	Slow/Static Beta Filter Value			Total Y Channels				Total X Channels			

- Bit 11: **Slow/Static Filter Enable**
  - 0: Slow/Static filter disabled
  - 1: Slow/Static filter enabled
- Bit 8-9: **Static Beta Filter Value**
  - 3-bit value
- Bit 4-7: **Total Y Channels**
  - 8-bit decimal value = number of channels
- Bit 0-3: **Total X Channels**
  - 8-bit decimal value = number of channels

Table A.23: X and Y Lower Calibration

Register: 0xB001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Lower Y Calibration								Lower X Calibration							

- Bit 8-15: **Lower Y Calibration**
  - 8-bit value
- Bit 0-7: **Lower X Calibration**
  - 8-bit value

Table A.24: X and Y Upper Calibration

Register: 0xB002

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Upper Y Calibration								Upper X Calibration							

- Bit 8-15: **Upper Y Calibration**
  - 8-bit value
- Bit 0-7: **Upper X Calibration**
  - 8-bit value

Table A.25: Bottom and Top Speed

Register: 0xB003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Top Speed								Bottom Speed							

- Bit 8-15: **Top Speed**
  - 8-bit value * 4ms
- Bit 0-7: **Bottom Speed**
  - 8-bit value

Table A.26: Channel Enable Mask

Register: 0xB006

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Please note that all channels in use must be selected
- Bit 0-9: Channel Enable Mask
  - 0: Disabled

- 1: Channel 0 enabled for trackpad
- 2: Channel 1 enabled for trackpad
- 4: Channel 2 enabled for trackpad
- 8: Channel 3 enabled for trackpad
- 16: Channel 4 enabled for trackpad
- 32: Channel 5 enabled for trackpad
- 64: Channel 6 enabled for trackpad
- 128: Channel 7 enabled for trackpad
- 256: Channel 8 enabled for trackpad
- 512: Channel 9 enabled for trackpad
- 1024: Channel 10 enabled for trackpad
- 2048: Channel 11 enabled for trackpad
- 4096: Channel 12 enabled for trackpad
- 8192: Channel 13 enabled for trackpad

Table A.27: Trackpad Enable Status Link

Register: 0xB007

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

› Bit 0-15: Enable Status Link
- 0x6EC (decimal = 1772): Output linked to channel prox
- 0x6EE (decimal = 1774): Output linked to channel touch

Table A.28: Delta Link

Register: 0xB008, 0xB009, 0xB00A, 0xB00B, 0xB00C, 0xB00D, 0xB00E, 0xB00F, 0xB010, 0xB011, 0xB012, 0xB013

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Delta Link															

› Bit 0-15: Delta Link - Select element order per channel
› Delta link number corresponds with slider element order
- 0x000 (decimal = 0): Disabled
- 0x430 (decimal = 1072): Channel 0 enabled for element
- 0x452 (decimal = 1106): Channel 1 enabled for element
- 0x474 (decimal = 1140): Channel 2 enabled for element
- 0x496 (decimal = 1174): Channel 3 enabled for element
- 0x4B8 (decimal = 1208): Channel 4 enabled for element
- 0x4DA (decimal = 1242): Channel 5 enabled for element
- 0x4FC (decimal = 1276): Channel 6 enabled for element
- 0x51E (decimal = 1310): Channel 7 enabled for element
- 0x540 (decimal = 1344): Channel 8 enabled for element
- 0x562 (decimal = 1378): Channel 9 enabled for element
- 0x584 (decimal = 1412): Channel 10 enabled for element
- 0x5A6 (decimal = 1446): Channel 11 enabled for element
- 0x5C8 (decimal = 1480): Channel 12 enabled for element
- 0x5EA (decimal = 1514): Channel 13 enabled for element

Table A.29: Trackpad Gestures 0

Register: 0xB014

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Minimum Gesture Time								Reserved			Strict X swipe	Strict Y swipe	Flick En	Swipe En	Tap En

› Bit 8-15: Minimum Gesture Time
- 8-bit value * 16 ms

› Bit 4: Strict X Swipe
- 0: X Swipe gesture valid if
  - X coordinate travel distance is greater than the specified Swipe Distance
  - X coordinate swipe occurs within the specified Maximum Swipe Time

- 1: X Swipe gesture valid if
  - X coordinate travel distance is greater than the specified Swipe Distance
  - X coordinate swipe occurs within the specified Maximum Swipe Time
  - X coordinate travel distance is at least twice the Y coordinate travel distance

Bit 3: Strict Y Swipe

- 0: Y Swipe gesture valid if
  - Y coordinate travel distance is greater than the specified Swipe Distance
  - Y coordinate swipe occurs within the specified Maximum Swipe Time
- 1: Y Swipe gesture valid if
  - Y coordinate travel distance is greater than the specified Swipe Distance
  - Y coordinate swipe occurs within the specified Maximum Swipe Time
  - Y coordinate travel distance is at least twice the X coordinate travel distance

Bit 2: Flick Enable

- Flick gesture disabled
- Flick gesture enabled

Bit 1: Swipe Enable

- Swipe gesture disabled
- Swipe gesture enabled

Bit 0: Tap Enable

- Tap gesture disabled
- Tap gesture enabled

Table A.30: Trackpad Gestures 1

Register: 0xB015

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Maximum swipe time								Maximum tap time							

Bit 8-15: Maximum Swipe Time

- 8-bit value * 16 ms

Bit 0-7: Maximum Tap Time

- 8-bit value * 16 ms

Table A.31: Tap Distance

Register: 0xB016

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tap distance															

Bit 0-15: Tap Distance

- 16-bit value (pxs)

Table A.32: Swipe Distance

Register: 0xB017

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Swipe distance															

Bit 0-15: Swipe Distance

- 16-bit value (pxs)

Table A.33: Output Port x Enable and Configuration Settings

Register: 0xC000, 0xC100, 0xC200

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved									OUTC	OUTB	Reserved		OUTA	Open Drain	Enable

Bit 6: OUTC

- 0: OUTC pin not linked to output port
- 1: OUTC pin linked to output port

› Bit 5: OUTB
- 0: OUTB pin not linked to output port
- 1: OUTB pin linked to output port

› Bit 2: TOUT0
- 0: OUTA pin not linked to output port
- 1: OUTA pin linked to output port

› Bit 1: Open Drain
- 0: Output port pins configured as push-pull with active high logic
- 1: Output port pins configured as open drain with active low logic

› Bit 0: Enable
- 0: Output port disabled
- 1: Output port enabled

Table A.34: Output Port x Channel Enable Mask

Register: 0xC001, 0xC101, 0xC201

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

› Please note that more than one channel can be selected as an output

› Bit 0-7: Channel Enable Mask
- 0: Disabled
- 1: Channel 0 enabled as output
- 2: Channel 1 enabled as output
- 4: Channel 2 enabled as output
- 8: Channel 3 enabled as output
- 16: Channel 4 enabled as output
- 32: Channel 5 enabled as output
- 64: Channel 6 enabled as output
- 128: Channel 7 enabled as output

› Bit 8-13: Channel Enable Mask
- 256: Channel 8 enabled as output
- 512: Channel 9 enabled as output
- 1024: Channel 10 enabled as output
- 2048: Channel 11 enabled as output
- 4096: Channel 12 enabled as output
- 8192: Channel 13 enabled as output

Table A.35: Output Port x Enable Status Link

Register: 0xC002, 0xC102, 0xC202

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

› Bit 0-15: Enable Status Link
- 0x061E (decimal = 1566): Output linked to trackpad gesture events
- 0x06E8 (decimal = 1768): Output linked to channel prox
- 0x06EA (decimal = 1770): Output linked to channel touch .
- 0x06F8 (decimal = 1784): Direct output

Table A.36: Control Settings

Register: 0xD0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

› Bit 6-7: **Interface Selection**
- 00: I^2C streaming
- 01: I^2C event mode
- 10: I^2C Stream in touch

› Bit 4-5: **Power Mode Selection**

- 00: Normal power
- 01: Low power
- 10: Ultra-low Power
- 11: Automatic power mode switching

› Bit 3: **Execute Reseed Command**
- 0: Do not reseed
- 1: Reseed

› Bit 2: **Execute ATI Command**
- 0: Do not ATI
- 1: ATI

› Bit 1: **Soft Reset**
- 0: Do not reset device
- 1: Reset device

› Bit 0: **Acknowledge Reset Command**
- 0: Do not acknowledge reset
- 1: Acknowledge reset

Table A.37: ULP Entry Mask

Register: 0xD9

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

› Bit 0-13: **ULP Entry Mask**
- Channel 0-13 mask to enable the device to enter ULP if the relevant channel is in activation.
- 0: If channel is in activation, device will not enter ULP
- 1: Device will be able to enter ULP even if channel is in activation,

Table A.38: Event Enable

Register: 0xDA

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Res	Track-pad	Reserved								Touch event	Prox event

› Bit 13: **Power Event**
- 0: Power event masked
- 1: Power event enabled

› Bit 12: **ATI Event**
- 0: ATI event masked
- 1: ATI event enabled

› Bit 10: **Trackpad Event**
- 0: Trackpad event masked
- 1: Trackpad event enabled

› Bit 1: **Touch Event**
- 0: Touch event masked
- 1: Touch event enabled

› Bit 0: **Prox Event**
- 0: Prox event masked
- 1: Prox event enabled

Table A.39: I^2C Communication

Register: 0xDB

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												Stop re-ceived	Start re-ceived	RW check dis-abled	Stop bit dis-abled

› Bit 3: **Stop Received Flag**
- 0: No I^2C stop received
- 1: I^2C stop received

› Bit 2: **Start Received Flag**
- 0: No I^2C start received

- 1: I²C start received

- Bit 1: **RW Check Disabled**
  - 0: Write not allowed on read only registers
  - 1: Read and write allowed on read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I²C communication window terminated by stop bit.
  - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window

Table A.40: Output Port Override

Register: 0xDC

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved													CH2	CH1	CH0

- Note: To write to this register, the register's address (0xDC) must be commanded explicitly before writing data i.e. in a separate I²C write setup command.
- Output port mask enable should have channel's 0/1/2 selected for the OUTx output override functionality to work
- Bit 2: **CH2**
  - 0: Channel 2 disabled as direct output
  - 1: Channel 2 enabled as direct output
- Bit 1: **CH1**
  - 0: Channel 1 disabled as direct output
  - 1: Channel 1 enabled as direct output
- Bit 0: **CH0**
  - 0: Channel 0 disabled as direct output
  - 1: Channel 0 enabled as direct output

Table A.41: I²C Communication Timeout

Register: 0xDD

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I²C Communication Timeout															

- Note: To write to this register, the register's address (0xDD) must be commanded explicitly before writing data i.e. in a separate I²C write setup command.
- Bit 0-16: **I²C Communication Timeout**
  - 16-bit value (ms) Range: 0 - 3276
  - Default = 500ms

B Revision History

Release	Date	Changes
v1.0	October 2021	Initial release
v1.1	September 2022	Updated output link pointers Updated Memory Map Minor formatting fixes
v1.2	January 2024	Firmware version updated to v1.2 Added order code 102 Changes implemented for IQS7222D 102 IC option according to "PIN-230172" Updated current consumption tables Updated channel options section Updated addressing information for order code 102 Updated power mode and mode timeout section Update Memory Map version information table Memory Map reserved bits corrected Updated force communication "t_{wait}" description Updated Output pin naming Added WLCSP18 package option
v1.3	February 2025	Updated the Order Code section.

Contact Information

	South Africa (Headquarters)	China
Physical Address	1 Bergsig Avenue Paarl 7646 South Africa	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC
Tel	+27 21 863 0033	+86 755 8303 5294 ext 808
Email	info@azoteq.com	info@azoteq.com

	USA	Taiwan
Physical Address	7000 North Mopac Expressway Suite 200 Austin TX 78731 USA	Xintai 5th Road, Sec. 1 No. 99, 9F-12C Xizhi District 221001 New Taipei City Taiwan
Tel	+1 512 538 1995	+886 932 219 444
Email	info@azoteq.com	info@azoteq.com

Visit www.azoteq.com
for a list of distributors and worldwide representation.

Patents as listed on www.azoteq.com/patents-trademarks/ may relate to the device or usage of the device.