IQS7229A DATASHEET

8 Channel Self-capacitive Touch and Proximity Controller with I²C communications interface, integrated noise immunity algorithms, and low power options

1 Device Overview

The IQS7229A ProxSense® IC is both a standalone and I²C sensing device for multi-channel proximity or touch sensing requirements. The sensor is fully I²C compatible, and on-chip calculations enable the IC to respond effectively even in the lowest power modes.

1.1 Main Features

- Highly flexible ProxSense® device
- 8 Self-Capacitive external sensor pad connections
- Configure up to 8 Channels using the external connections
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & Hysteresis
- Built-in Signal processing options:
  - 6 Standalone touch output pins for a robust output in a noisy environment
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY
- Standalone, event, and streaming modes
- Effective response times for critical trigger requirements
  - Proximity: 177 ms
  - Touch: 216 ms
- Supply Voltage 1.71V to 3.5V
- Small package
  - QFN20 (3.00 x 3.00 x 0.55 mm) - 0.40 mm pitch

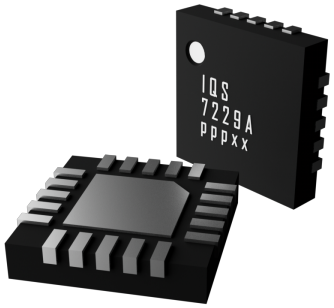


Figure 1.1: QFN20

1.2 Applications

- Appliance user interface (Buttons)
- Low power Wake-up Buttons/Proximity
- Door open/close switch

1.3 Block Diagram

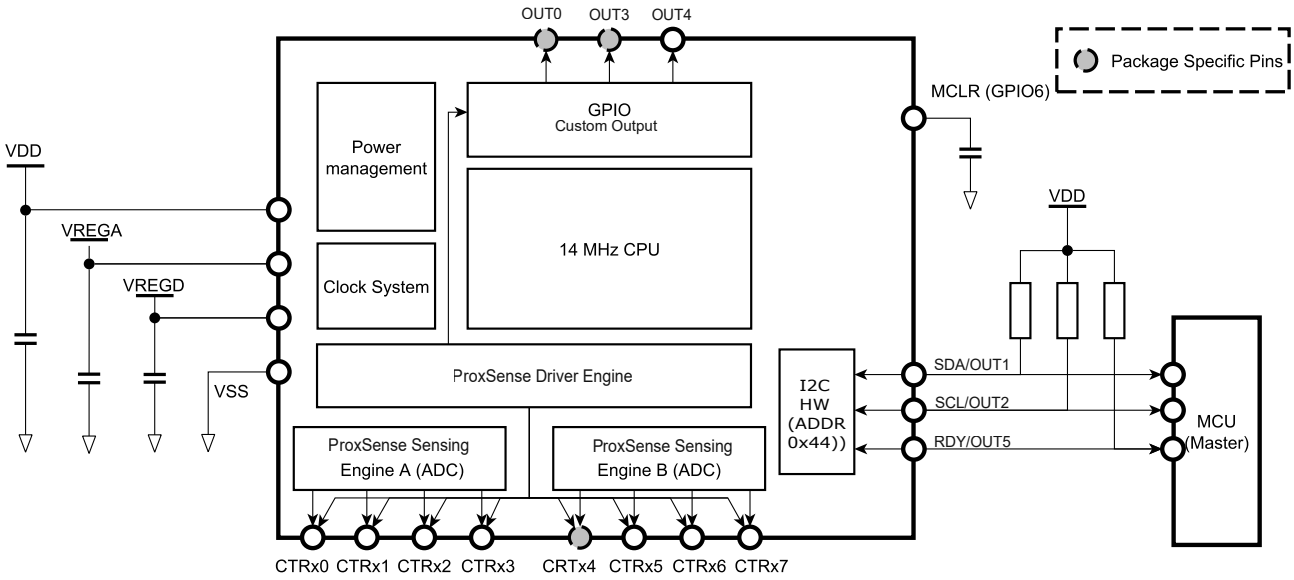


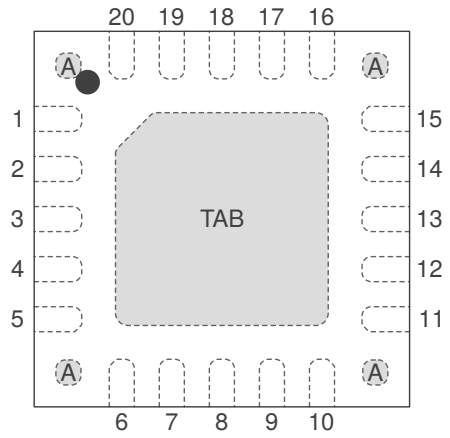
Figure 1.2: Functional Block Diagram

Contents

2 Hardware Connection

2.1 QFN20 Pin Diagram

Table 2.1: 20-pin QFN Package (Top View)



Top View

Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6
2	VREGD	12	CRx7
3	VSS	13	Vbias
4	VREGA	14	Output0
5	CRx0	15	Output3
6	CRx1	16	Output4
7	CRx2	17	RDY/Output5
8	CRx3	18	SCL/Output2
9	CRx4	19	SDA/Output1
10	CRx5	20	MCLR

Area name	Signal name
TAB[i]	Thermal pad (floating)
A[ii]	Thermal pad (floating)

2.2 Pin Attributes

Table 2.2: Pin Attributes

Pin no. QFN20	Signal name	Signal type	Buffer type	Power source
1	VDD	Power	Power	N/A
2	VREGD	Power	Power	N/A
3	VSS	Power	Power	N/A
4	VREGA	Power	Power	N/A
5	CRx0	Analog		VREGA
6	CRx1	Analog		VREGA
7	CRx2	Analog		VREGA
8	CRx3	Analog		VREGA
9	CRx4	Analog		VREGA
10	CRx5	Analog		VREGA
11	CRx6	Analog		VREGA
12	CRx7	Analog		VREGA
13	Vbias	Analog		VREGA
14	Output0	Digital		VDD
19	SDA/Output1	Digital		VDD
18	SCL/Output2	Digital		VDD
15	Output3	Digital		VDD
16	Output4	Digital		VDD
17	RDY/Output5	Digital		VDD
20	MCLR	Digital		VDD

[i] It is recommended to connect the thermal pad (TAB) to VSS.
[ii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Signal Descriptions

Table 2.3: Signal Descriptions

Function	Signal name	Pin no. QFN20	Pin type[iii]	Description
ProxSense®	CRx0	5	IO	ProxSense® channel
	CRx1	6	IO	
	CRx2	7	IO	
	CRx3	8	IO	
	CRx4	9	IO	
	CRx5	10	IO	
	CRx6	11	IO	
	CRx7	12	IO	
	Vbias	13	O	Vbias pad
GPIO	Output0	14	IO	Output0 pad
	Output3	15	IO	Output3 pad
	Output4	16	IO	Output4 pad
	RDY/Output5	17	IO	RDY/Output5 pad
	MCLR	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA/Output1	19	IO	I^2C data
	SCL/Output2	18	IO	I^2C clock
Power	VDD	1	P	Power supply input voltage
	VREGD	2	P	Internal regulated supply output for digital domain
	VSS	3	P	Analog/digital ground
	VREGA	4	P	Internal regulated supply output for analog domain

[iii] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.4 Reference Schematic

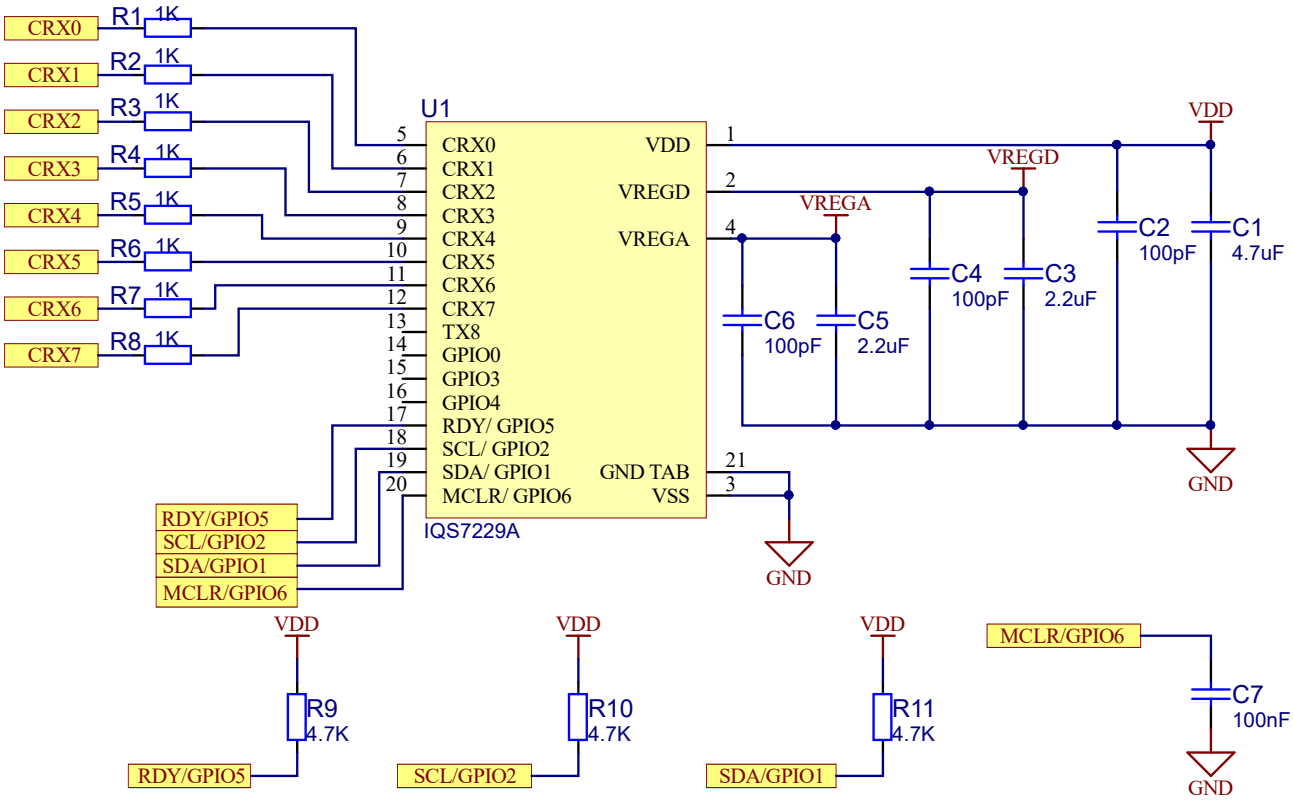


Figure 2.1: 8 Button Self-Capacitance Reference Schematic

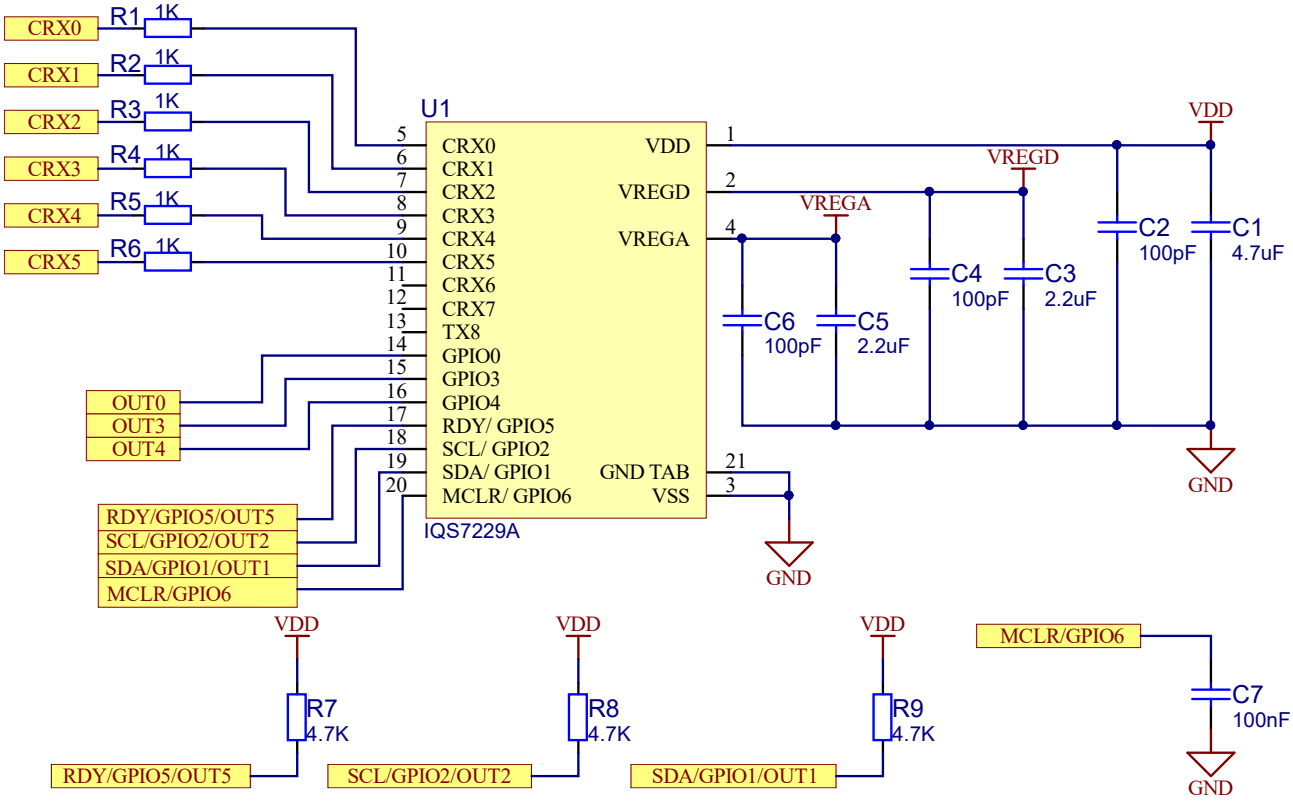


Figure 2.2: 6 Button Self-Capacitance Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxSense® pin (referenced to VSS)	−0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	−0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	−40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	−40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxSense® blocks (self-capacitance mode)	1		400[ii]	pF
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iii]	0.47	10[iv]	kΩ

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.

[ii] RCx = 0 Ω.

[iii] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[iv] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6\times F_{xfer})}$ where C is the pin capacitance to VSS.

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[v]	±4000	V

3.4 Current Consumption

Sensing Mode: : Self-Capacitive
Number of Channels : 8 (I^2C) / 6 (Standalone)
Number of Cycles : 4
ATI Target : 512
ATI Base : 112
HFosc : 14 MHz
Charge transfer frequency : 500 kHz
Interface Selection : Event Mode / Standalone

Table 3.4: Typical Current Consumption

Power Mode	Report rate (sampling rate) [ms]	Typical current [µA]	
		Eight channel I^2C - Event mode	Six channel standalone
Normal power / low-power	15	600	545
	20	517	460
	25	428	380
	50	209	185
	100	107	94
	150	72	63
	300	37	33
	500	23	20

[v] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

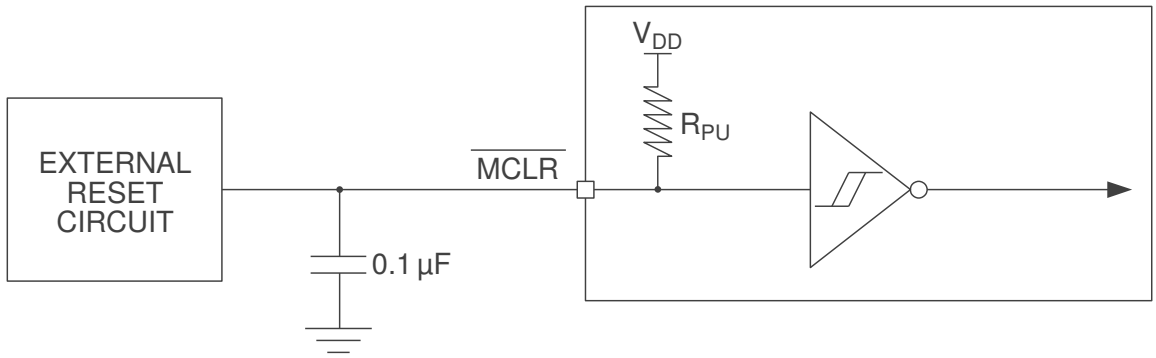


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

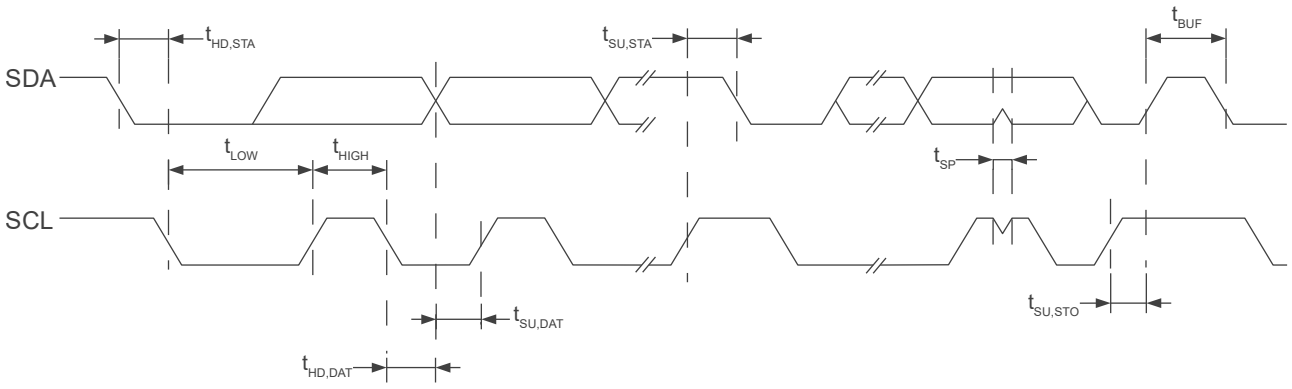


Figure 4.2: I²C Mode Timing Diagram

[i] Refers to Output0, Output3, Output4, and RDY/Output5 pins.

5 ProxSense® Module

The IQS7229A contains dual ProxSense® modules that use patented technology to measure and process the sensor data. Two modules ensure a robust response from multi-channel implementations. The multiple touch and proximity outputs are the primary output from the sensor.

5.1 Channel Options

Self-capacitance design is possible with the IQS7229A.

- Sensor pad design overview: AZD125

5.2 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance, and all outputs are derived from this.

5.2.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *Maximum Counts*. If the ATI setting or hardware causes the measured count values to be higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.3 Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.3.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations that would call for a manual reseed. A reseed takes the latest measured counts and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (*Control Settings*, bit 3).

5.4 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxSense® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

5.5 Automatic Re-ATI

5.5.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7229A, a status bit will set momentarily to indicate that this has occurred.

5.5.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.16.

$$\text{Re-ATI Boundary} = \text{ATI Target} \pm \left(\frac{1}{8} \times \text{ATI Target}\right) \quad (1)$$

For example, assume that the ATI target is configured to 800 and that the default boundary value is 1/8 * 800 = 100. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\text{LTA} > 900 \text{ or } \text{LTA} < 700$$

The ATI algorithm executes in a short time, so it goes unnoticed by the user.

5.5.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation ≥ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set *ATI Error*. The flag status is only updated again when a new ATI algorithm is performed.

Note: Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable timeout (*ATI Error Timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI from repeating indefinitely. An ATI error should, however, not occur under normal circumstances.

5.6 Channel Outputs

5.6.1 Channel Proximity

A channel proximity event occurs when the channel proximity threshold has been reached. For a capacitive sensor, this occurs when a user's finger or a conductive object comes into close proximity with the sensor. A channel proximity output is debounced (see Table A.11), and the proximity threshold configured is a delta value (see Table A.11) measuring how much a channel's count value has deviated from the reference/LTA value.

5.6.2 Channel Touch

A channel touch event occurs when the touch threshold has been reached. Touch threshold can be calculated as:

$$\text{Threshold} = \text{value} \times \frac{\text{LTA}}{256} \tag{2}$$

Here *value* refers to the value entered into the register, and *threshold* refers to the number that is calculated from the *value* and subsequently compared to the count delta to determine whether there is a touch event. The touch hysteresis value determines the corresponding touch release threshold. Release threshold can be calculated as:

$$\text{Release threshold} = \frac{\text{LTA}}{256} \times (\text{Threshold value - Hysteresis value}) \tag{3}$$

Here both *threshold value* and *hysteresis value* are configurable parameters in the memory map, and *release threshold* is calculated from these values and compared to the count delta to determine whether a touch event should be cleared.

6 Sensing Modes

6.1 Power Mode and Mode Timeout

The IQS7229A offers 2 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP

In order to optimise power consumption and performance, power modes are "stepped" by default in order to move to power-efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout". The value for the power mode to never timeout (i.e., the current power mode will never progress to a lower power mode), is 0x00.

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitised raw input offers various damping options as defined in Tables A.14 and A.15.

$$\text{Damping factor} = \frac{\text{Beta}}{256} \tag{4}$$

7 Hardware Settings

Settings specific to hardware and the ProxSense® Module charge transfer characteristics can be changed.

Note: Below, some are described, while the other hardware parameters are not discussed as they should only be adjusted under the guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters will be provided. For high-resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate that a reset event occurred. This bit is cleared when the master sets the *Ack Reset*; if it becomes set again, the master will know a reset has occurred, and can react appropriately.

While the *Reset* bit remains set:

- The device will not be able to enter into I^2C Event mode operation (i.e., streaming communication behaviour will be maintained until the Reset bit is cleared).
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

7.2.2 Software Reset

The IQS7229A can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design-specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 Automated Start-up

The device is programmed with the application firmware, bundled with settings specifically configured for the current hardware as described in Section 8.1. After power-up, the device will automatically use the settings and perform the configuration/setup accordingly.

8.3 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software-triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.

Note: In order to keep the WDT effective and active, the IQS7229A must not be used in a low power mode (bits 4-5 of Table A.21), where it is in a sleep mode.

8.4 RF Immunity

The IQS7229A has immunity to high-power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100 pF in parallel with the 2.2 µF ceramic on V_{REG}. Place a 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470 Ω–1 kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two-wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7229A supports the following:

- *Fast-mode-plus* standard I²C up to 1 MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7229A implements 8-bit addressing with 2 data bytes at each address, with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The 7-bit device address for order code 000 is 0x44 (’01000100’). The full address byte for address 0x44 will thus be 0x89 (read) or 0x88 (write).

Other address options exist on special requests. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement a 16-bit addressing scheme.

9.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to only address each Block as an 8-bit address, and then continue to clock into the next address locations. For example, if the procedure depicted below is followed, you will read the values from the hypothetical address 0xE000 to 0xE300:

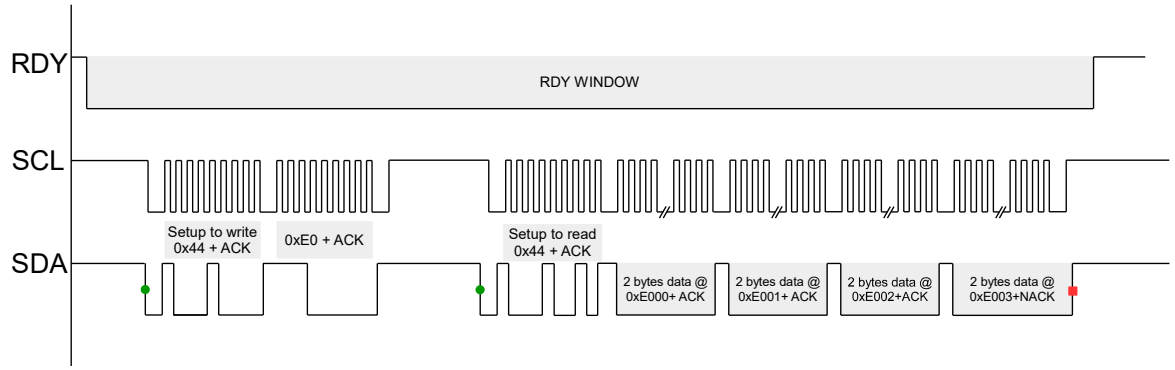


Figure 9.1: Extended 16-bit Addressing for Continuous Block

However, if you need to address a specific byte in that extended memory map space, then you will need to address using the full 16-bit address:

Note: The 16-bit address is high byte first, unlike the data, which is low byte first.

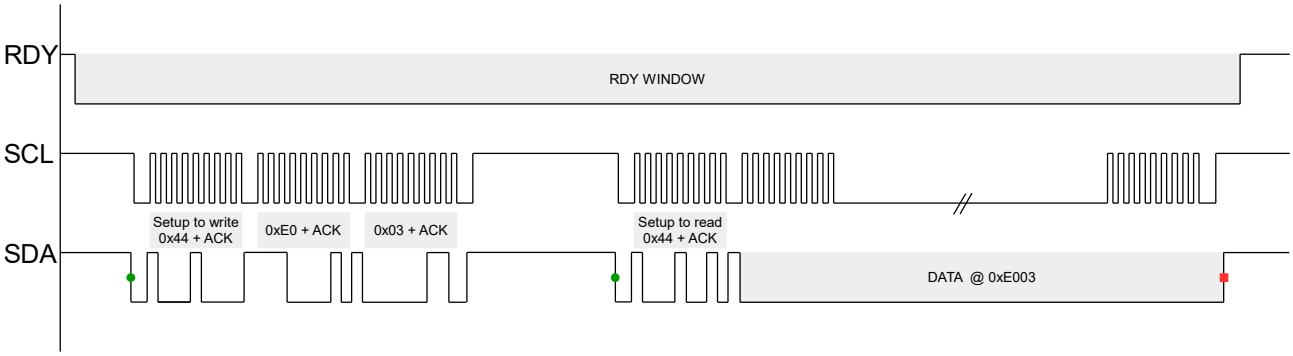


Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, and then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

The h file generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively –in a single block of data or the entire memory map, refer to Figure 9.1, or data can be written explicitly to a specific address, refer to Figure 9.2. An example of the h file exported by the GUI and the order of the data is shown in Figure 9.3 below.

```
/* Change the Sensor 0 Settings */
/* Memory Map Position 0x30 - 0x39 */
#define SENSOR_0_SETUP_0
#define SENSOR_0_SETUP_1
```

Start address
0x01 → LSB
0x07 → MSB

Figure 9.3: Example of an H file Exported by the GUI

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive; however, the corresponding data was missed or lost, and this should be avoided. The default I²C timeout period is set to 500 ms and can be adjusted in register 0xD9.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0xD8) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

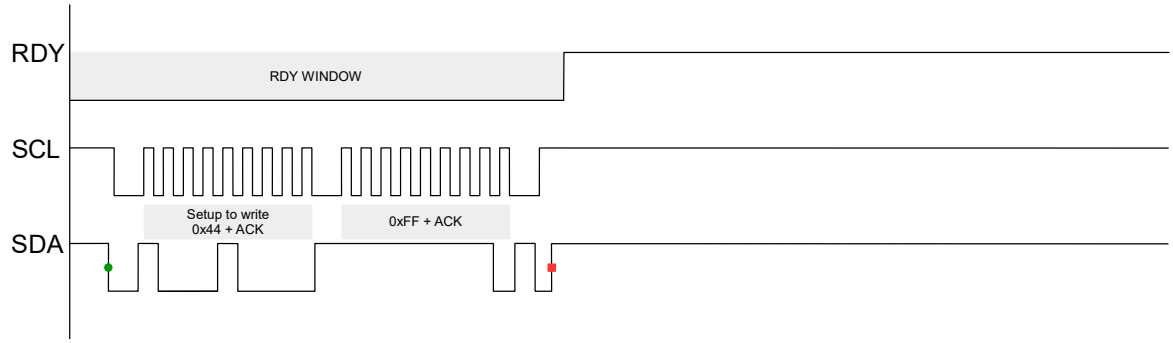


Figure 9.4: Force Stop Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep, allowing wake-up from the touch device when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e., while RDY = high).

9.10 I²C Interface

The IQS7229A has 3 I²C *interface options*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0xD4* (normal power) and register *0xD6* (low power), respectively.

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurrs. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.10.3 I²C Stream in Touch Mode

Stream in Touch is a hybrid I²C mode between streaming mode and event mode. The device follows event mode I²C protocol but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I²C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

9.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *Events* register 0x11 to ensure all event flags are cleared; otherwise, continuous reporting (RDY interrupts) will persist after every conversion cycle, similar to streaming mode.

9.11.1 Events

Numerous events can be individually enabled to trigger communication; bit definitions can be found in Tables A.3 and A.2:

- ATI error
- ATI Event
- Power event
- Touch event
- Proximity event

9.11.2 Force Communication

In streaming mode, the IQS7229A I²C will provide Ready (RDY) windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7229A should only be initiated in a Ready window, but a communication request described in Figure 9.5 below will force a Ready window to open. In event mode, Ready windows are only provided when an event is reported, and a Ready window must be requested to write or read settings outside of this window. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}) is application-specific, but the average values are 0.1 ms $\leq t_{wait} \leq$ 20 ms[i].

The communication request sequence is shown in Figure 9.5 below.

[i] Please contact Azoteq for an application specific value of t_{wait}

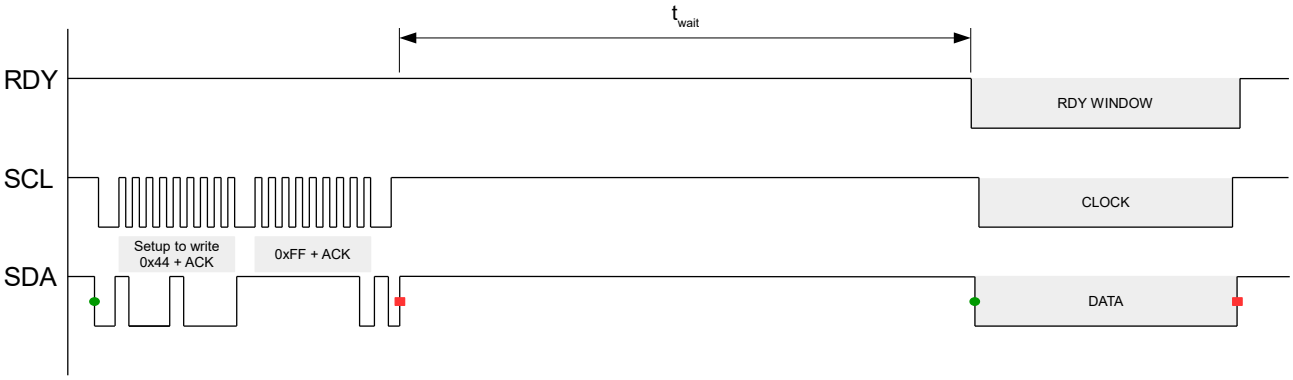


Figure 9.5: Force Communication Sequence

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions.

Address	Data (16-bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only	**System Flags**	
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Prox Event States	See Table A.4
0x13	Touch Event States	See Table A.5
Read Only	**Channel Counts**	
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
Read Only	**Channel LTA**	
0x30	Channel 0 LTA	16-bit value
0x31	Channel 1 LTA	
0x32	Channel 2 LTA	
0x33	Channel 3 LTA	
0x34	Channel 4 LTA	
0x35	Channel 5 LTA	
0x36	Channel 6 LTA	
0x37	Channel 7 LTA	
Read Only	**Channel Raw Counts**	
0x40	Channel 0 Raw Counts - f_0	16-bit value
0x41	Channel 0 Raw Counts - f_1	
0x42	Channel 0 Raw Counts - f_2	
0x43	Channel 1 Raw Counts - f_0	
0x44	Channel 1 Raw Counts - f_1	
0x45	Channel 1 Raw Counts - f_2	
0x46	Channel 2 Raw Counts - f_0	
0x47	Channel 2 Raw Counts - f_1	
0x48	Channel 2 Raw Counts - f_2	
0x49	Channel 3 Raw Counts - f_0	
0x4A	Channel 3 Raw Counts - f_1	
0x4B	Channel 3 Raw Counts - f_2	
Read-Write	**Cycle Setup**	
0x8000	Cycle 0 Setup	See Table A.6
0x8001		See Table A.7
0x8100	Cycle 1 Setup	See Table A.6
0x8101		See Table A.7
0x8200	Cycle 2 Setup	See Table A.6
0x8201		See Table A.7
0x8300	Cycle 3 Setup	See Table A.6
0x8301		See Table A.7
0x8400	Global Cycle Setup	See Table A.8
0x8401	Coarse and Fine Divider Preloads	See Table A.9

0x8402	Compensation Preload	See Table A.9
Read-Write	**Button Setup - Thresholds, Hysteresis, Debounce and Beta Filter**	
0x9000	Button 0 Setup	See Table A.11
0x9001		See Table A.12
0x9002		See Table A.13
0x9003		See Table A.14
0x9004		See Table A.15
0x9100	Button 1 Setup	See Table A.11
0x9101		See Table A.12
0x9102		See Table A.13
0x9103		See Table A.14
0x9104		See Table A.15
0x9200	Button 2 Setup	See Table A.11
0x9201		See Table A.12
0x9202		See Table A.13
0x9203		See Table A.14
0x9204		See Table A.15
0x9300	Button 3 Setup	See Table A.11
0x9301		See Table A.12
0x9302		See Table A.13
0x9303		See Table A.14
0x9304		See Table A.15
0x9400	Button 4 Setup	See Table A.11
0x9401		See Table A.12
0x9402		See Table A.13
0x9403		See Table A.14
0x9404		See Table A.15
0x9500	Button 5 Setup	See Table A.11
0x9501		See Table A.12
0x9502		See Table A.13
0x9503		See Table A.14
0x9504		See Table A.15
0x9600	Button 6 Setup	See Table A.11
0x9601		See Table A.12
0x9602		See Table A.13
0x9603		See Table A.14
0x9604		See Table A.15
0x9700	Button 7 Setup	See Table A.11
0x9701		See Table A.12
0x9702		See Table A.13
0x9703		See Table A.14
0x9704		See Table A.15
Read-Write	**Channel Setup- ATI Parameters, Reference Channel and Rx Select**	
	Channel 0	
0xA000	CRX Select and General Channel Setup	See Table A.16
0xA001	ATI Base and Target	See Table A.18
0xA002	Fine and Coarse Multipliers	See Table A.19
0xA003	ATI Compensation	See Table A.20
	Channel 1	
0xA100	CRX Select and General Channel Setup	See Table A.16
0xA101	ATI Base and Target	See Table A.18
0xA102	Fine and Coarse Multipliers	See Table A.19

0xA103	ATI Compensation	See Table A.20
	Channel 2	
0xA200	CRX Select and General Channel Setup	See Table A.16
0xA201	ATI Base and Target	See Table A.18
0xA202	Fine and Coarse Multipliers	See Table A.19
0xA203	ATI Compensation	See Table A.20
	Channel 3	
0xA300	CRX Select and General Channel Setup	See Table A.16
0xA301	ATI Base and Target	See Table A.18
0xA302	Fine and Coarse Multipliers	See Table A.19
0xA303	ATI Compensation	See Table A.20
	Channel 4	
0xA400	CRX Select and General Channel Setup	See Table A.17
0xA401	ATI Base and Target	See Table A.18
0xA402	Fine and Coarse Multipliers	See Table A.19
0xA403	ATI Compensation	See Table A.20
	Channel 5	
0xA500	CRX Select and General Channel Setup	See Table A.17
0xA501	ATI Base and Target	See Table A.18
0xA502	Fine and Coarse Multipliers	See Table A.19
0xA503	ATI Compensation	See Table A.20
	Channel 6	
0xA600	CRX Select and General Channel Setup	See Table A.17
0xA601	ATI Base and Target	See Table A.18
0xA602	Fine and Coarse Multipliers	See Table A.19
0xA603	ATI Compensation	See Table A.20
	Channel 7	
0xA700	CRX Select and General Channel Setup	See Table A.17
0xA701	ATI Base and Target	See Table A.18
0xA702	Fine and Coarse Multipliers	See Table A.19
0xA703	ATI Compensation	See Table A.20
Read Only	**Global Reference LTA**	
0xB0	System Reference LTA	16-bit value
0xB1	Raw Counts Re-ATI Threshold	
0xB2	Beta Upper Bound	
Read-Write	**PMU and System Settings**	
0xD0	Control settings	See Table A.21
0xD1	ATI Error Timeout	16-bit value * 0.5 (s)
0xD2	ATI Report Rate	16-bit value (ms)
0xD3	Normal Power Mode Timeout	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	16-bit value (ms)
0xD5	Reserved	16-bit value (ms)
0xD6	Low Power Mode Report Rate	16-bit value (ms)
0xD7	Event Enable	See Table A.22
0xD8	Communication Timeout	See Table A.23
0xD9	I^2C Communication	See Table A.24
Read-Write	**Calcap Settings**	
0xE0	Calcap Settings	See Table A.25

11 Implementation and Layout

11.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

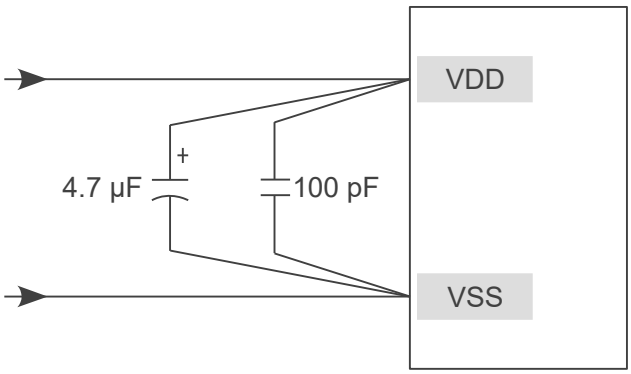


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 11.2 below shows an example placement of the VREG capacitors.

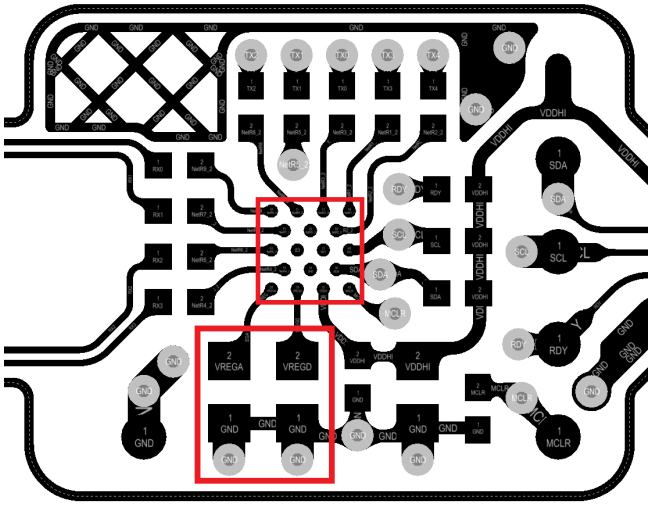


Figure 11.2: VREG Capacitor Placement Close to IC

12 Ordering Information

12.1 Ordering Code

IQS7229A zzz ppb

Table 12.1: Order Code Description

IC NAME				IQS7229A
POWER-ON CONFIGURATION	zzz	=	100 101	8-button, configurable via I²C[i]. 6-button standalone
PACKAGE TYPE	pp	=	QN QF	QFN-20 package QFN-20 package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

12.2 Top Marking

12.2.1 QFN20 Package Marking Option (IQS7229AzzzQNR)

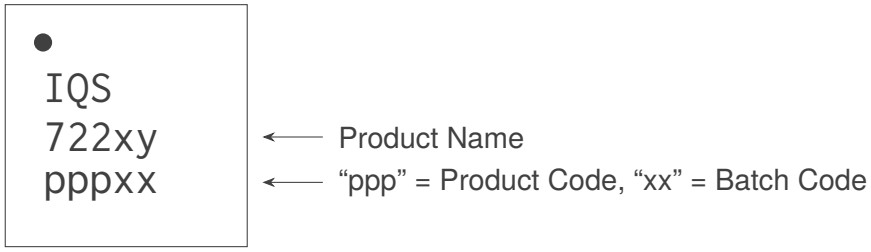


Figure 12.1: IQS722xy-QFN20 Package Top Marking

12.2.2 QFN20 Package Marking Option (IQS7229AzzzQFR)

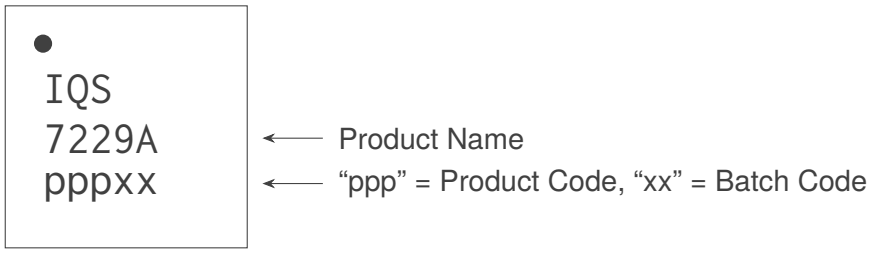


Figure 12.2: IQS7229A-QFN20 Package Top Marking

[i] I²C address = 0x44

13 Package Specification

13.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

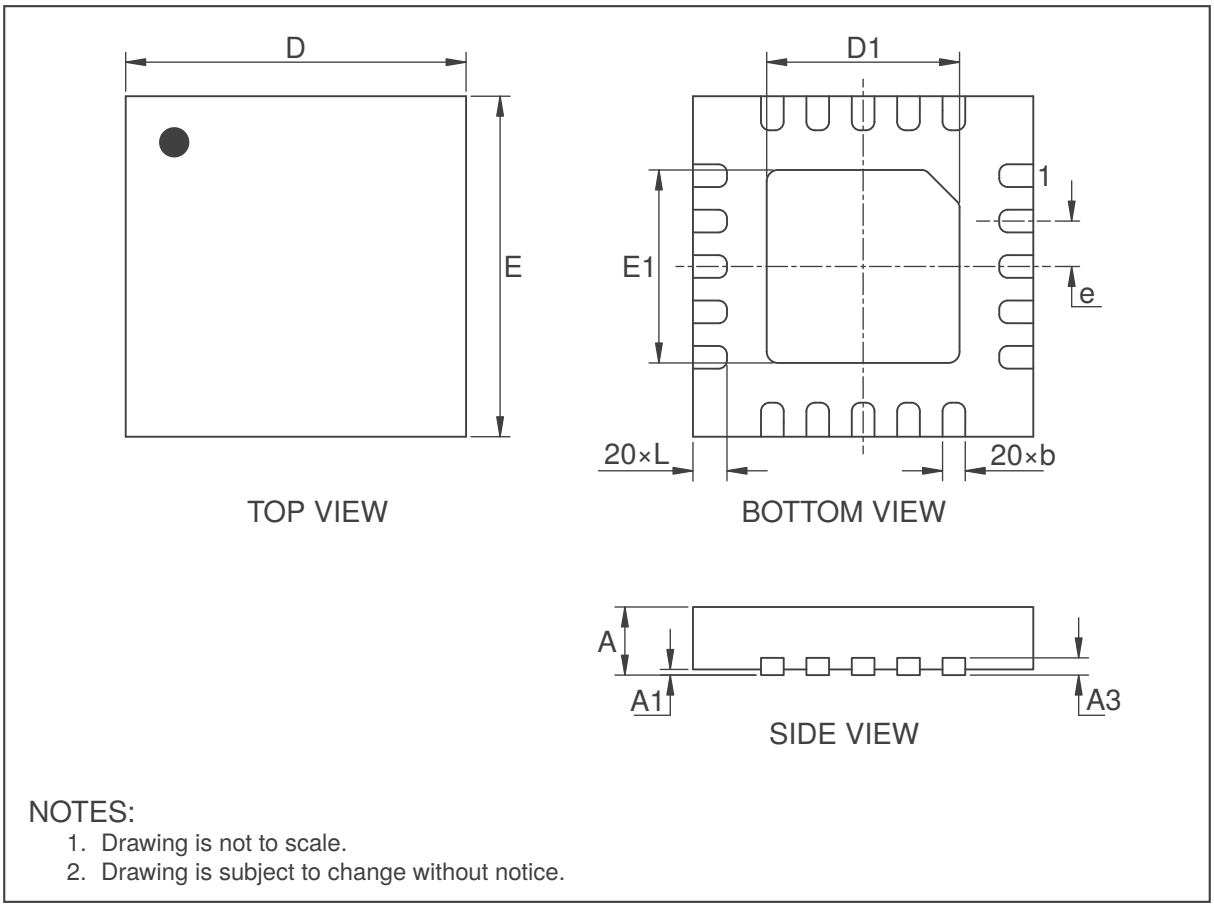
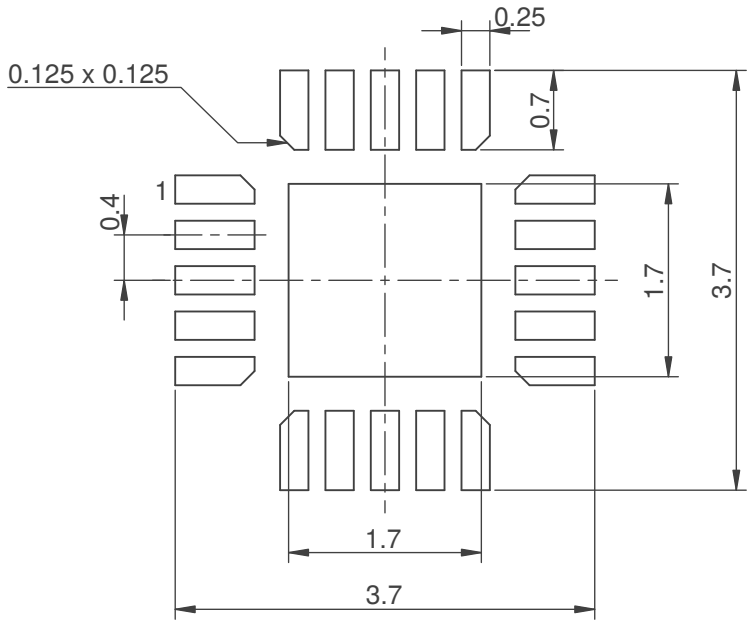


Figure 13.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

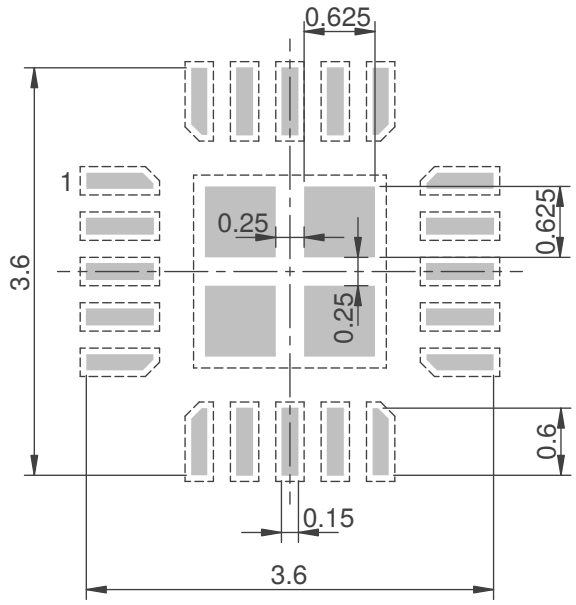
Table 13.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

13.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: QFN (3x3)-20 (QFR) Recommended Footprint

13.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

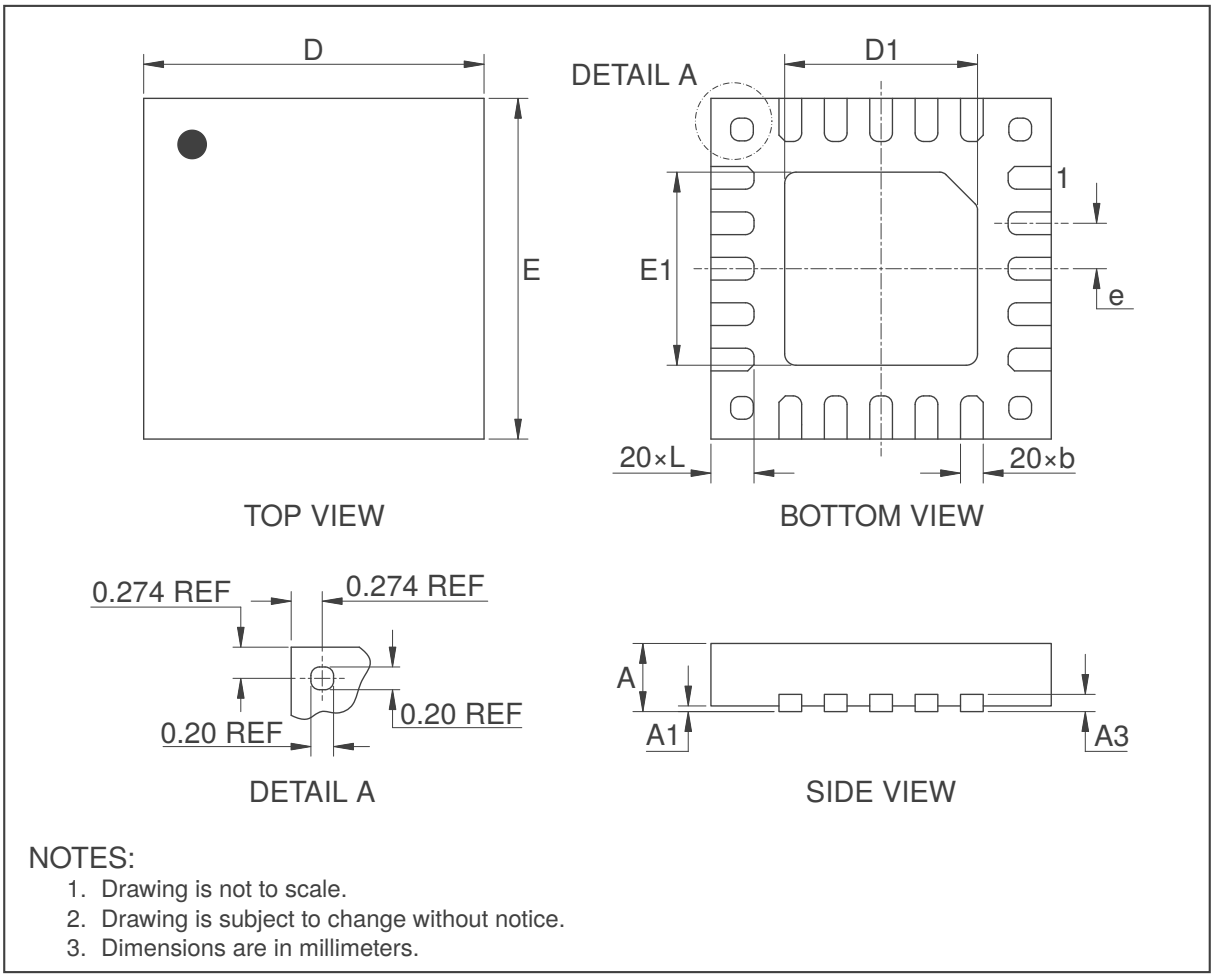
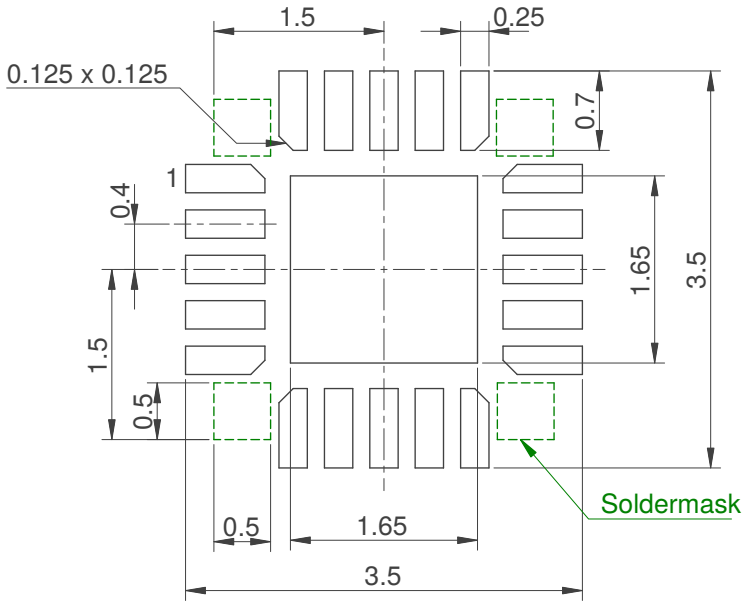


Figure 13.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

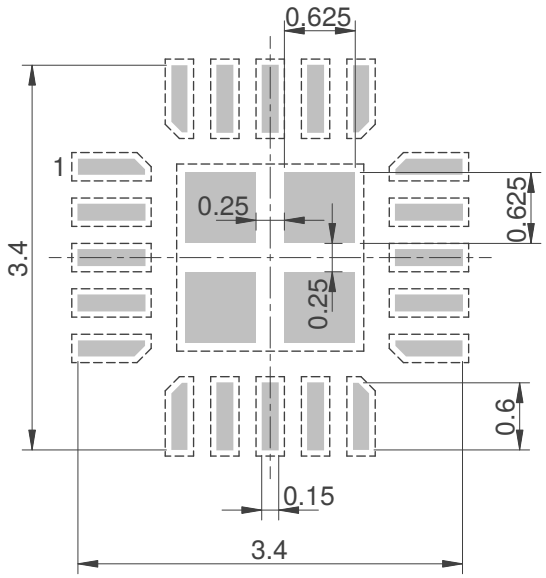
Table 13.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

13.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



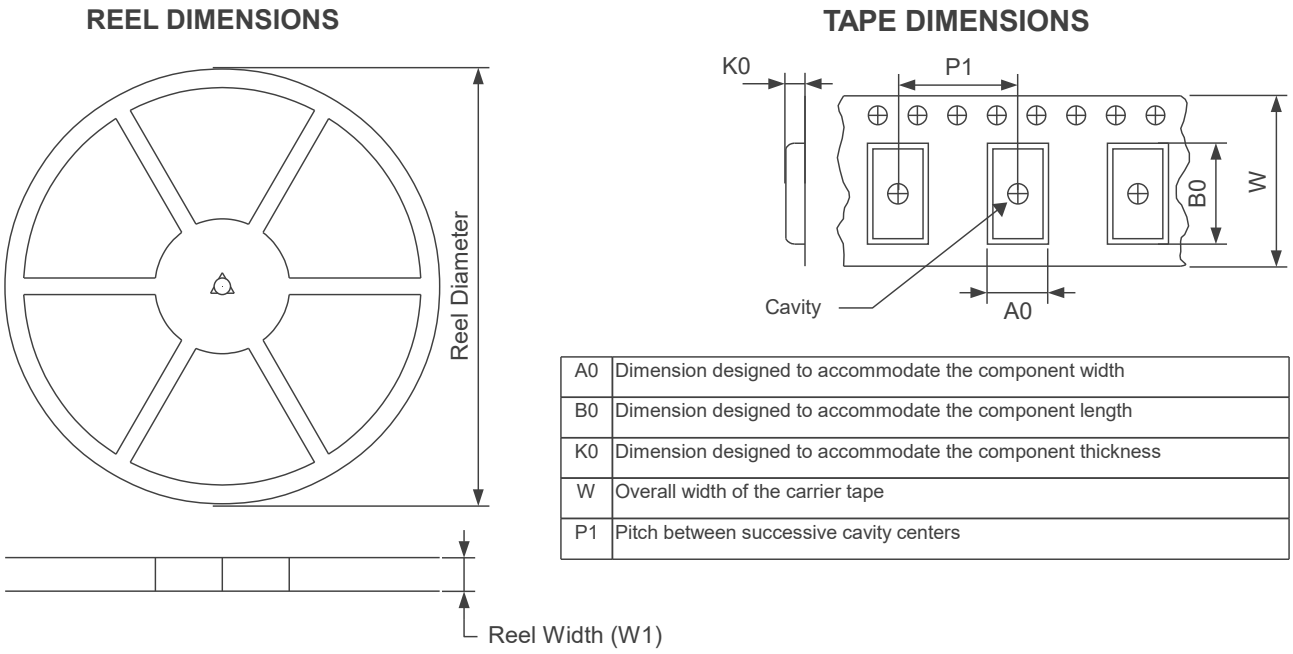
RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 13.4: QFN (3x3)-20 (QNR) Recommended Footprint

13.5 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 13.5: Tape and Reel Specification

Table 13.3: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

13.6 Moisture Sensitivity Levels

Table 13.4: Moisture Sensitivity Levels

Package	MSL
QFN20	1

13.7 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

A.1 Version Information (0x00 – 0x09)

Note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Address	Category	Name	Value	Order Code
0x00	Application Version Information	Product Number	2055	100 (I^2C) 101 (Standalone)
0x01		Major Version	1	
0x02		Minor Version	0	
0x03		Patch Number (commit hash)	Reserved	
0x04				
0x05	ROM Library Version Information	Library Number	Reserved	
0x06		Major Version		
0x07		Minor Version		
0x08		Patch Number (commit hash)	Reserved	
0x09				

A.2 System Status (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Global Halt	Reserved	Power Mode		Reset	Reserved	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 4-5: **Current Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

A.3 Events (0x11)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Power Event	ATI Event	Reserved			

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

A.4 Proximity Event States (0x12)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

A.5 Touch Event States (0x13)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

A.6 Cycle Setup 0

(0x8000, 0x8100, 8200, 8300)

Bit	15	14	13	12	11	10	9	8
Description	Conversion Frequency Period							

Bit	7	6	5	4	3	2	1	0
Description	Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - The calculation of the charge transfer frequency (f_{xfer}) is shown below. The relevant formula is determined by the value of the dead time enabled bit (refer to Table A.7)
  - Dead time disabled: $f_{xfer} = \frac{f_{clk}}{2 \times period + 2}$
  - Dead time enabled: $f_{xfer} = \frac{f_{clk}}{2 \times period + 3}$
  - Range: 0 - 127
- Bit 0-7: **Conversion Frequency Fraction**

- $256 \times \frac{f_{conv}}{f_{clk}}$
- Range: 0 - 255

› **Note:** If Conversion frequency fraction is fixed at 127 and dead time is enabled, the following values of the conversion period will result in the corresponding charge transfer frequencies:
  - 1: 2 MHz
  - 5: 1 MHz
  - 12: 500 kHz
  - 17: 350 kHz
  - 26: 250 kHz
  - 53: 125 kHz

A.7 Cycle Setup 1

(0x8001, 0x8101, 8201, 8301)

Bit	15	14	13	12	11	10	9	8
Description	CRX7	CRX6	CRX5	CRX4	CRX3	CRX2	CRX1	CRX0

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Ground Inactive Rxs	Dead Time Enabled	Reserved			

› Bit 15: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled

› Bit 14: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled

› Bit 13: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled

› Bit 12: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled

› Bit 11: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled

› Bit 10: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled

› Bit 9: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled

› Bit 8: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled

› Bit 5: **Ground Inactive Rx's**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded

› Bit 4: **Dead Time Enabled**
  - Functionality used to avoid transient effect.
  - 0: Deadtime disabled
  - 1: Deadtime enabled

A.8 Global Cycle Setup (0x8400)

Bit	15	14	13	12	11	10	9	8
Description	0	Maximum counts		0	1	0	1	1

Bit	7	6	5	4	3	2	1	0
Description	1	0	0	0	Reserved		1	1

- Bit 13-14: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384

A.9 Coarse And Fine Multipliers Preload (0x8401)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Divider Preload					Reserved

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Coarse Divider Preload				

- Bit 0-4: **Coarse Divider Preload**
  - Setting a default coarse mirror value will ensure that the set base value is reached on startup.
  - 5-bit coarse divider preload value
- Bit 9-13: **Fine Divider Preload**
  - Setting a default fine mirror value will ensure that the set base value is reached on startup.
  - 5-bit fine divider preload value

A.10 ATI Compensation Preload (0x8402)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						ATI Compensation Preloac	

Bit	7	6	5	4	3	2	1	0
Description	ATI Compensation Preload							

- Bit 0-9: **ATI Compensation Preload**
  - Setting a default compensation value will ensure that the set target value is reached on startup.
  - 10-bit preload value

A.11 Button Setup 0

(0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700)

Bit	15	14	13	12	11	10	9	8
Description	Exit Debounce Value				Enter Debounce Value			

Bit	7	6	5	4	3	2	1	0
Description	Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled

- 4-bit value

› Bit 8-11: **Enter Debounce Value**
- 0000: Debounce disabled
- 4-bit value

› Bit 0-7 : **Proximity Threshold**
- 8 -bit value

A.12 Button Setup 1

(0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701)

Bit	15	14	13	12	11	10	9	8
Description	Touch Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Touch Threshold							

› Bit 8-15: **Touch Hysteresis**
- Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:

$$\frac{\text{LTA} \times \text{Threshold bit value}}{2^8} - \frac{\text{Threshold bit value} \times \text{Hysteresis bit value} \times \text{LTA}}{2^{16}}$$

› Bit 0-7: **Touch Threshold**
- $\frac{\text{LTA}}{256} \times$ 8-bit value

A.13 Button Setup 2

(0x9002, 0x9102, 0x9202, 0x9302, 0x9402, 0x9502, 0x9602, 0x9702)

Bit	15	14	13	12	11	10	9	8
Description	Touch Event Timeout							

Bit	7	6	5	4	3	2	1	0
Description	Prox Event Timeout							

› Bit 8-15: **Touch Event Timeout**
- 8-bit value * 500 ms where a reseed of the LTA is forced. If the LTA is outside of the LTA ATI band a re-ATI event will occur if ATI is not disabled
- 0: Never timeout

› Bit 0-7: **Prox Event Timeout**
- 8-bit value * 500 ms where a reseed of the LTA is forced. If the LTA is outside of the LTA ATI band a re-ATI event will occur if ATI is not disabled
- 0: Never timeout

A.14 Filter Betas

(0x9003, 0x9103, 0x9203, 0x9303, 0x9403, 0x9503, 0x9603, 0x9703)

Bit	15	14	13	12	11	10	9	8
Description	LTA Low Power Beta Filter Value				LTA Normal Power Beta Filter Value			

Bit	7	6	5	4	3	2	1	0
Description	Counts Low Power Beta Filter Value				Counts Normal Power Beta Filter Value			

› Bit 12-15: **LTA Low Power Beta Filter Value**
- 4-bit value

› Bit 8-11: **LTA Normal Power Beta Filter Value**

- 4-bit value

› Bit 4-7: **Counts Low Power Beta Filter Value**
- 4-bit value

› Bit 0-3: **Counts Normal Power Beta Filter Value**
- 4-bit value

A.15 Fast Filter Betas

(0x9004, 0x9104, 0x9204, 0x9304, 0x9404, 0x9504, 0x9604, 0x9704)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	LTA Low Power Fast Beta Filter Value				LTA Normal Power Fast Beta Filter Value			

› Bit 4-7: **LTA Low Power Fast Beta Filter Value**
- 4-bit value

› Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
- 4-bit value

A.16 CRX Select And General Channel Setup (CH0-CH3)

(0xA000, 0xA100, 0xA200, 0xA300)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		ATI Band		Global Halt	Reserved		Channel Enabled

Bit	7	6	5	4	3	2	1	0
Description	CRx3	CRx2	CRx1	CRx0	Cs Size	Vref 0.5V Enable	Reserved	

› Bit 12-13: **ATI band**
- 00: 1/16 * Target
- 01: 1/8 * Target
- 10: 1/4 * Target
- 11: 1/2 * Target

› Bit 11: **Global halt**
- If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
- 0: Halt disabled
- 1: Halt enabled

› Bit 8: **Channel Enabled**
- 0: Channel disabled
- 1: Channel enabled

› Bit 7: **CRx3**
- 0: CRx3 disabled
- 1: CRx3 enabled

› Bit 6: **CRx2**
- 0: CRx2 disabled
- 1: CRx2 enabled

› Bit 5: **CRx1**
- 0: CRx1 disabled
- 1: CRx1 enabled

› Bit 4: **CRx0**
- 0: CRx0 disabled
- 1: CRx0 enabled

› Bit 3: **Cs Size**

- 0: 40 pF - use when external load is very small
- 1: 80 pF

› Bit 2: **Vref 0.5 V Enable**
- Decrease internal sampling capacitor size
- 0: Vref 0.5 V disabled - C_s = Value chosen in Cs 80 pF bit (40 pF / 80 pF)
- 1: Vref 0.5 V enabled - C_s = Half of the value chosen in Cs 80pF bit (40 pF / 80 pF)

A.17 CRX Select And General Channel Setup (CH4-CH7)

(0xA400, 0xA500, 0xA600, 0xA700)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		ATI Band		Global Halt	Reserved		Channel Enabled

Bit	7	6	5	4	3	2	1	0
Description	CRx7	CRx6	CRx5	CRx4	Cs Size	Vref 0.5 V Enable	Reserved	

› Bit 12-13: **ATI band**
- 00: 1/16 * Target
- 01: 1/8 * Target
- 10: 1/4 * Target
- 11: 1/2 * Target

› Bit 11: **Global halt**
- If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
- 0: Halt disabled
- 1: Halt enabled

› Bit 8: **Channel Enabled**
- 0: Channel disabled
- 1: Channel enabled

› Bit 7: **CRx7**
- 0: CRx7 disabled
- 1: CRx7 enabled

› Bit 6: **CRx6**
- 0: CRx6 disabled
- 1: CRx6 enabled

› Bit 5: **CRx5**
- 0: CRx5 disabled
- 1: CRx5 enabled

› Bit 4: **CRx4**
- 0: CRx4 disabled
- 1: CRx4 enabled

› Bit 3: **Cs Size**
- 0: 40 pF - use when external load is very small
- 1: 80 pF

› Bit 2: **Vref 0.5 V Enable**
- Decrease internal sampling capacitor size
- 0: Vref 0.5 V disabled - C_s = Value chosen in Cs 80 pF bit (40 pF / 80 pF)
- 1: Vref 0.5 V enabled - C_s = Half of the value chosen in Cs 80 pF bit (40 pF / 80 pF)

› Bit 0-1: **Projected Bias Select**
- 00: 2 µA
- 01: 5 µA
- 10: 7 µA
- 11: 10 µA

A.18 ATI Base And Target

(0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601, 0xA701)

Bit	15	14	13	12	11	10	9	8
Description	ATI Target							

Bit	7	6	5	4	3	2	1	0
Description	ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

A.19 Fine And Coarse Multipliers

(0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602, 0xA702)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Fractional Divider					Coarse Fractional Multiplier

Bit	7	6	5	4	3	2	1	0
Description	Coarse Fractional Multiplier			Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

A.20 ATI Compensation

(0xA003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603, 0xA703)

Bit	15	14	13	12	11	10	9	8
Description	Compensation Divider					Reserved	Compensation Selection	

Bit	7	6	5	4	3	2	1	0
Description	Compensation Selection							

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

A.21 Control Settings (0xD0)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Sampling Frequency Set

Bit	7	6	5	4	3	2	1	0
Description	Interface Selection		Power Mode Selection		Execute Reseed Command	Execute ATI Command	Soft Reset	Acknowledge Reset Command

- Bit 8: **Sampling Frequency Set**
  - This Setting is used to improve the performance of the system when a noisy frequency band is encountered during sampling
  - This setting is checked after every complete sampling cycle, that is, after sampling with all frequencies in the selected frequency set
  - 0: Set A – default frequency set
  - 1: Set B – alternate frequency set
- Bit 6-7: **Interface Selection**
  - 00: I²C streaming
  - 01: I²C event mode
  - 10: I²C Stream in touch
  - 11; Standalone
- Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device after communication window terminates
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

A.22 Event Enable (0xD7)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Power Event	ATI Event	Reserved			

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Touch Event	Proximity Event

- Bit 13: **Power Event**
  - 0: Power event masked
  - 1: Power event enabled
- Bit 12: **ATI Event**
  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 1: **Touch Event**
  - 0: Touch event masked

- 1: Touch event enabled

› Bit 0: **Prox Event**
- 0: Prox event masked
- 1: Prox event enabled

A.23 I2C Communication Timeout (0xD8)

Bit	15	14	13	12	11	10	9	8
Description	I2C Communication Timeout							

Bit	7	6	5	4	3	2	1	0
Description	I2C Communication Timeout							

› Bit 0-15: **I²C Communication Timeout**
- 16-bit value [ms]
- Range: 0 - 64535
- Default = 500 ms

A.24 I²C Communication (0xD9)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Stop Received Flag	Start Received Flag	RW Check Disabled	Stop Bit Disabled

› Bit 3: **Stop Received Flag**
- 0: No I²C stop received
- 1: I²C stop received

› Bit 2: **Start Received Flag**
- 0: No I²C start received
- 1: I²C start received

› Bit 1: **RW Check Disabled**
- 0: Write not allowed to read only registers
- 1: Read and write allowed to read only registers

› Bit 0: **Stop Bit Disabled**
- 0: I²C communication window terminated by stop bit.
- 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window.

A.25 Calibration Capacitor (0xE0)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Calcap Size			Calcap Status

› Bit 4: **Reserved**
- Set to 0

› Bit 1 - 3: **Calibration Capacitor Size**
- 000: None
- 001: 0.5 pF

- 010: 1.0 pF
- 011: 1.5 pF
- 100: 2.0 pF
- 101: 2.5 pF
- 110: 3.0 pF
- 111: 3.5 pF

- Bit 0: **Calibration Capacitor Status**
  - 0: Calibration capacitor disabled
  - 1: Calibration capacitor enabled

B Revision History

Release	Date	Changes
v1.0	December 2024	Initial release
v1.1	February 2025	Bit 4 of register 0xE0 marked as reserved

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